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Edition 1.0 2015-03

TECHNICAL SPECIFICATION

SPECIFICATION TECHNIQUE

colour inside

Device embedded substrate – Part 2-3: Guidelines – Design guide

Substrat avec appareil(s) intégré(s) – Partie 2-3: Directives – Guide de conception

IEC TS 62878-2-3:2015-03(en-fr)

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DEVICE EMBEDDED SUBSTRATE –

Part 2-3: Guidelines – Design guide

FOREWORD

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Technical Specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC TS 62878-2-3, which is a Technical Specification, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Specification is based on the following documents:

Enquiry draft	Report on voting
91/1143/DTS	91/1164A/RVC

Full information on the voting for the approval of this Technical Specification can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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INTRODUCTION

This part of IEC 62878 provides guidance with respect to device embedded substrate, fabricated by embedding discrete active and passive electronic devices into one or multiple inner layers of a substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Within the IEC 62878 series,

- IEC 62878-1-1 specifies the test methods,
- IEC TS 62878-2-1 gives a general description of the technology,
- IEC TS 62878-2-3, provides guidance on design, and
- IEC TS 62878-2-4 specifies the test element groups.

The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of the IEC 62878 series is to achieve a common understanding with respect to structures, test methods, design and fabrication processes and the use of the device embedded substrate in industry.

DEVICE EMBEDDED SUBSTRATE –

Part 2-3: Guidelines – Design guide

1 Scope

This part of IEC 62878 describes the design guide of device embedded substrates.

The design guide of device embedded substrate is essentially the same as that of various electronic circuit boards. This part of IEC 62878 enables a thorough understanding of circuit design, structure design, board design, board manufacturing, jisso (assembly processes) and tests of products.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

3 Terms, definition and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

3.2 Abbreviations

AABUS	as agreed between user and supplier
BGA	ball grid array
IPD	integrated passive device
LGA	land grid array
LSI	large scale integration
MEMS	micro electro mechanical systems
OSP	organic solderability preservative
SMD	surface mount device
TAB	tape automated bonding
WLP	wafer level package

4 Structure of device embedded substrates

4.1 General

The name of each part of a device embedded substrate is specified in Clause 4 to assist technical understanding of the structure and to avoid misinterpretation by engineers working in the relevant industry sectors.

4.2 Specification of the top and bottom surfaces of a device embedded substrate

The definition of the top and bottom surfaces of a device embedded substrate depends on the number of devices mounted on the surface of the substrate, as shown in Figure 1. The surface on which more components are mounted is the top surface. If a substrate is mounted on a printed wiring board (hereafter referred to as mother board), the surface of the substrate connecting to the wiring board is defined as the bottom surface even if it contains more input/output terminals (pads) (see Figure 2). If the design of the top and bottom surfaces has been AABUS, this agreement takes priority, even if it differs from the definition stated in this part of IEC 62878.

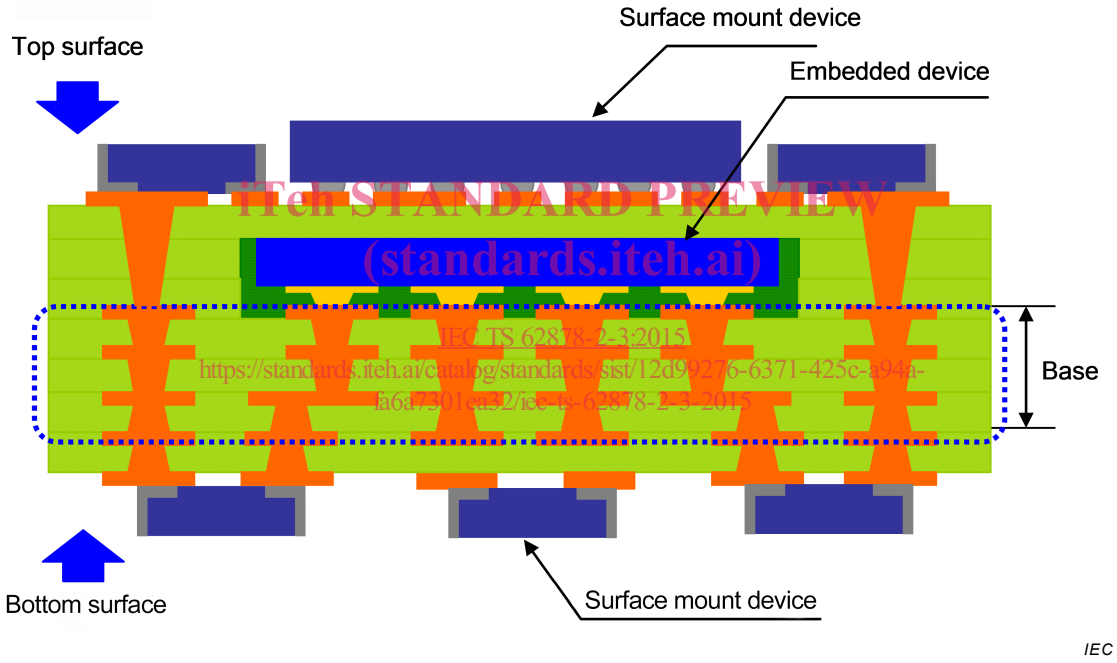


Figure 1 – Definition of top and bottom surfaces of a device embedded substrate

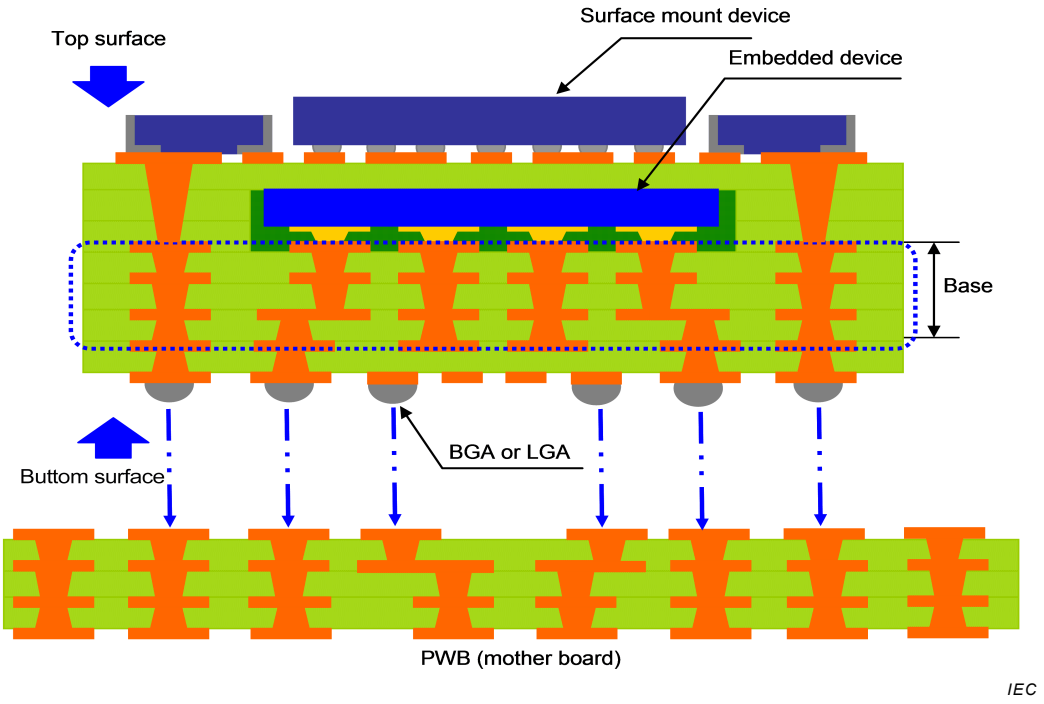
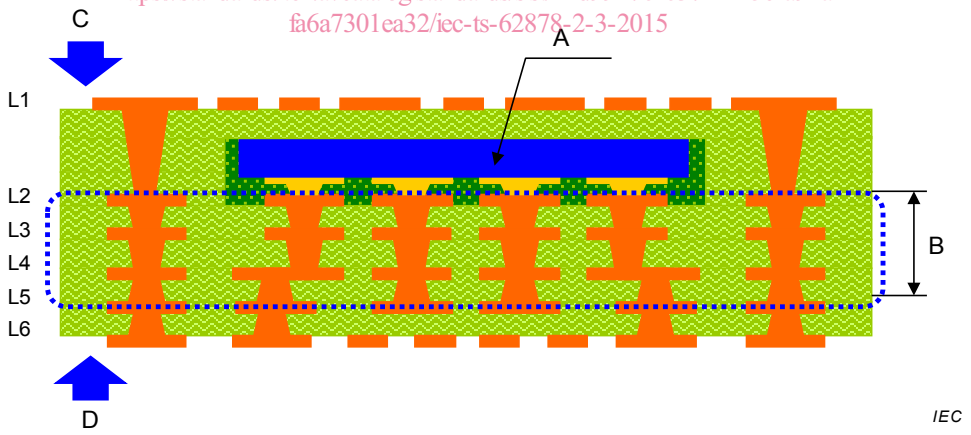


Figure 2 – Definition of top and bottom surfaces for mounting on a mother board

4.3 Definition of layers of a device embedded substrate

Names and symbols of layers in a device embedded board are illustrated in Figure 3. Each layer is numbered as L1, L2 to L6 (in case of 6 layers) from the top surface. The number indicates the order of the layer with respect to the top surface.



Key

A	Embedded component	C	Top surface
B	Base	D	Bottom surface

Figure 3 – Names of layers in pad connection

In the case of via connection, the position of connecting terminals of the embedded device is different from the surrounding layer number. The component symbol and connecting position(s) are defined as illustrated in Figure 4 in order to clarify the interconnecting positions of the embedded device and of its electrical terminals with respect to construction design, pattern design, board fabrication and jisso (assembly).

It is recommended to use the component symbols and names as shown in a circuit diagram to use 2 to 4 indications. The position of interconnection in the case of die-bonding or mounting

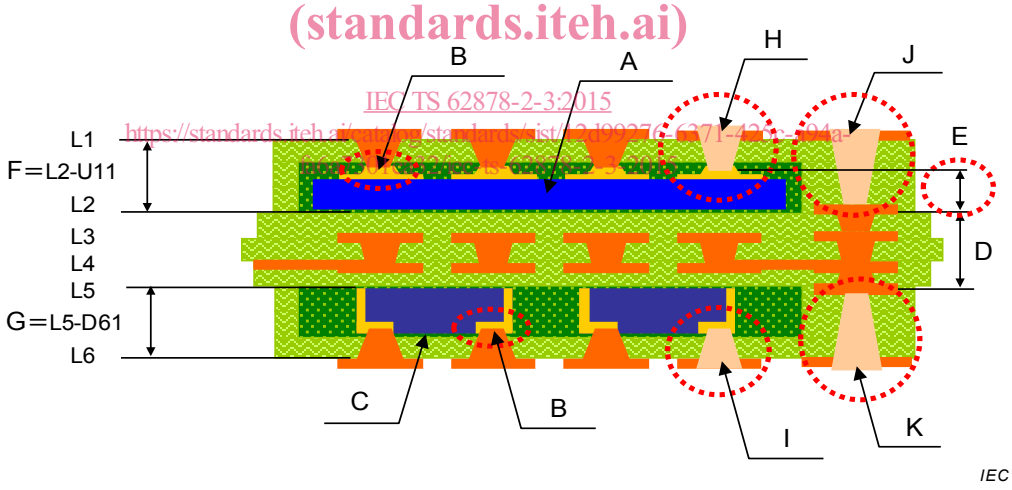
of a device embedded device may be expressed using another name in addition to the name of the layer in which the device is embedded.

The surface of a device is upward facing. Use upward (U) when connecting terminals are in the upward facing surface, and downward (D) when the terminals are in the downward facing surface.

A three digit number is used if multiple components are embedded and/or multiple connection terminals are in the same layer. The left side number indicates the interconnecting layer number and the right side number indicates the layer position of the embedded component. If there are multiple layers involved, numbers 1, 2 indicate the layers from the top for upward and numbers 1, 2 indicate the layers from the bottom for downward. The second number may be omitted if there is only one embedded component in a layer. See the example in Figure 4.

Figure 4 shows additional information on the interconnection position. The active device is mounted on the L2 layer and connected to the first layer with upward direction. In this case the name of the interconnection layer is expressed as L2-U11. The last digit 1 indicates the number of the embedded component. Passive components mounted on the L5 layer are connected to L6 with downward direction. In this case, the name of the interconnection layer is expressed as L5-D61.

A virtual layer is used as a virtual conductor layer and as the connecting points. The terminal connection design of an embedded device is carried out by first establishing the connection and hole machining data A and B, then the connection and hole machining data C and D for L2 and L5 (in the case of the above structure). The terminal setting may be omitted if a via connection and the positions of embedded device terminals and the conduction layer are the same.

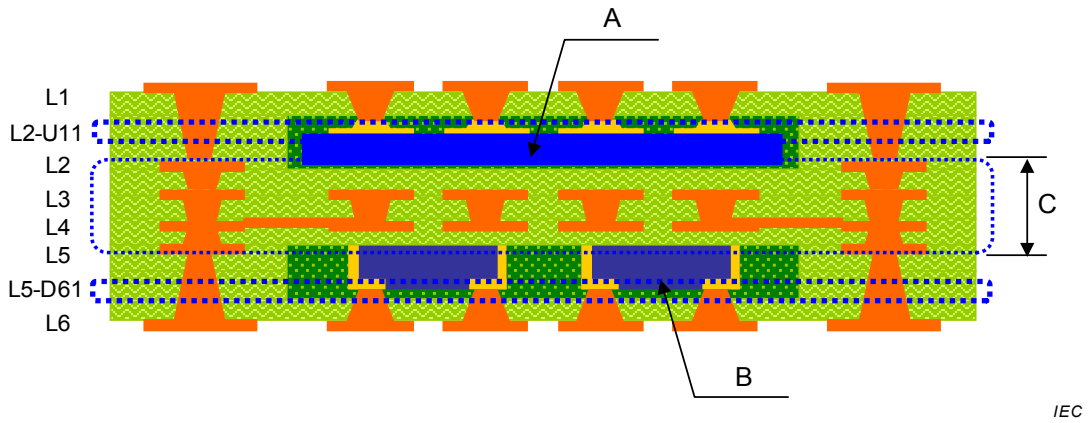


A	Embedded active device	G	Name of the layer between L5 and L6
B	Connecting terminal	H	Connection and machining data from L1 to a virtual layer (L2-U11)
C	Embedded passive device	I	Connection and machining data from L6 to a virtual layer (L5-D61)
D	Base	J	Connection and machining data from L1 to L2
E	Terminal position	K	Connection and machining data from L6 to L5
F	Name of the layer between L1 and L2		

Figure 4 – Additional information concerning the interconnection position

Figure 5 shows the interconnection position. Active device (xxxx) is mounted on the L2 layer and connected to the first layer with upward direction. In this case, the name of the interconnection position is expressed as xxxx-L2-U11. Passive components (yyyy) mounted

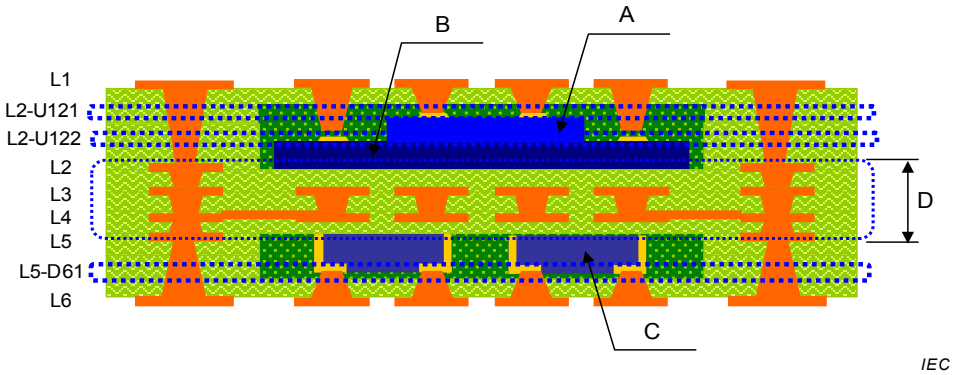
on the L5 layer are connected to L6 with downward direction. In this case, the name of the interconnection position is expressed as yyyy-L5-D61.



A	Embedded active device	C	Base
B	Embedded passive device		

Figure 5 – Names of layers in via connection [I]

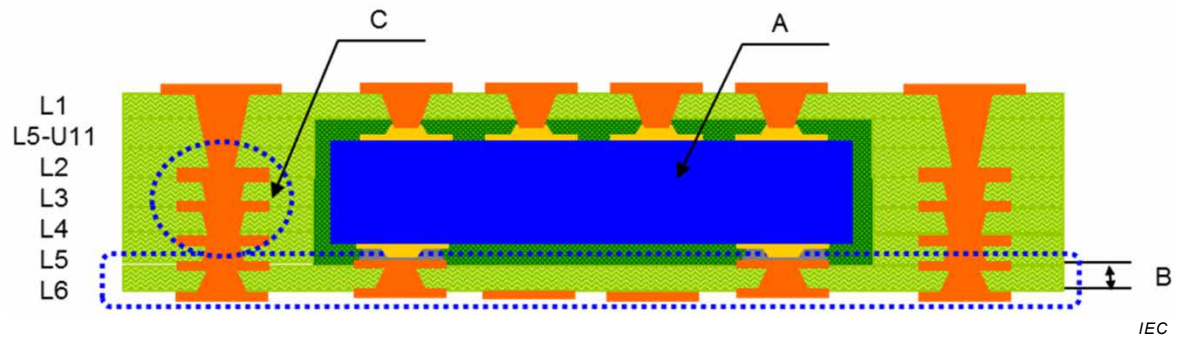
Figure 6 shows a chip-stacked case. Active device 2 (xxx2) is mounted on the L2 layer and active device 1 (xxx1) is stacked on active device 2. Both are connected to the L1 layer with upward direction. In this case the name of the interconnection position of active device 2 is expressed as xxx2-L2-U122. The name of the interconnection position of active device 1 is expressed as xxx1-L2-U121. The second digit from the right (2) shows the number of the embedded device.



A	Embedded active device 1	C	Embedded passive device
B	Embedded active device 2	D	Base

Figure 6 – Names of layers in via connection [II]

Figure 7 shows the interconnection position of an active device having multilayer connecting pads. Active device (xxxx) is mounted and connected to the L5 layer and pads on the other side are connected to the L1 layer with upward direction. Therefore, in this case, the name of the interconnection position of the active device is expressed as xxxx-L5-U11.



A	Embedded active device
B	Base
C	Conductor layer in embedding layer

Figure 7 – Names of layers in via connection [III]

The content of Figure 4 toFigure 7 is summarized in Table 1.

Table 1 – Name of layers of device embedded board

Example	Embedded device				Embedding and connection of embedded device					
	Device		Component number		Layer		Terminal direction	Layer	No. of components	
									No.	Layer
Figure 4	Active	-	A12	-	L2	-	U	1	1	Omit
	Passive	-	1	-	L5	-	D	6	1	Omit
Figure 5	Active	-	A13	-	L2	-	U	1	1	Omit
	Passive	-	2	-	L5	-	D	6	1	Omit
Figure 6	Active	-	A13	-	L2	-	U	1	2	1
	IPD	-	4	-	L2	-	U	1	2	2
	Capacitor	-	1	-	L5	-	D	6	1	Omit
Figure 7	IPD, etc.	-	12	-	L2	-	U	1	1	Omit
		-	B1	-	L6	-	D	6	1	Omit
Information on embedded components is necessary in embedded board design. For example, in Figure 4 the interconnection position of active device A12 is expressed as A12-L2-U11.										

4.4 Conductor spacing at a terminal

Subclause 4.4 defines the insulation layer thickness, the conductor spacing and the distance between electrode and conductor spacing at a terminal. Conductor spacing is hereafter referred to as electrode.

The insulation layer thickness and the distance between each conductive layer are defined with respect to the position of each layer, as follows:

a) The insulation layer thickness is defined as the layer separating the conductors. The thickness is not the thickness of each layer to be laminated but the thickness of the actual insulation layer of the substrate.

b) The conductor spacing is defined as the distance between conductors formed on one layer.

c) The spacing between the electrode and conductor is the thickness of the insulator between the terminals of the embedding device and the conductor layer to be connected.

d) The following terms are used to indicate each distance:

1) insulation layer thickness DG1 (dielectric gap);
2) spacing between conductor layers LG1 (layer gap);
3) spacing between terminal and conductor EG11 (device embedding gap).

The number used in the indication is the number of layers. The left number in 3) designates the conductor layer and the number on the right shows the step (first, second, etc.) of multi-device embedding into the substrate. See 4.3 for the definition of steps (layers).

Figure 8 and Figure 9 show definition of layers of a device embedded substrate for pad and via connections. Additional remarks are added to Figure 10 and Figure 11 for dielectric gap, layer gap and device embedding gap.

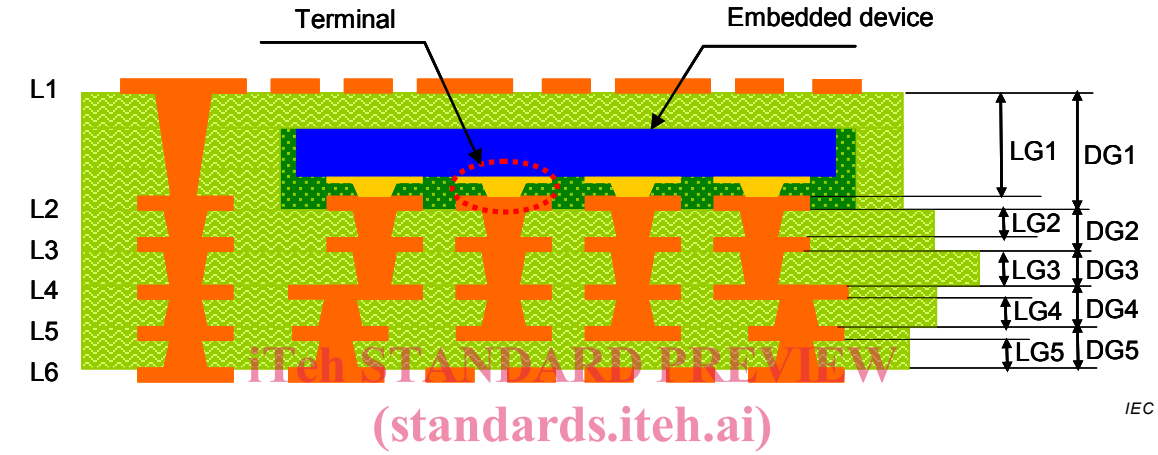


Figure 8 – Definitions of dielectric gap and layer gap in the pad connection method

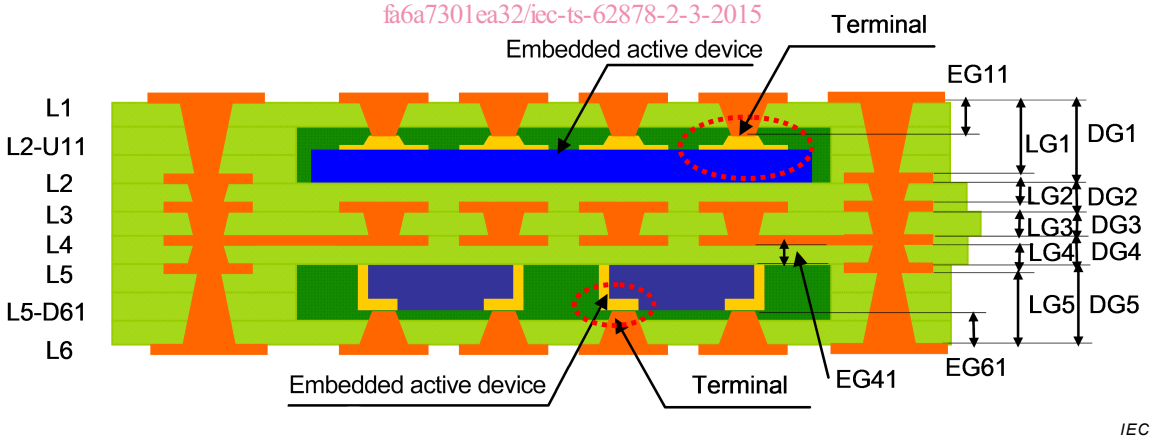


Figure 9 – Definitions of dielectric gap and layer gap in the via connection method