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Digital Test Interchange Format (DTIF)

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Contents

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FOREWORD

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
IEEE Std 1445-1998	93/321/FDIS	93/328/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The IEC Technical Committee and IEEE Technical Committee have decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IEEE Standard for Digital Test Interchange Format (DTIF)

Sponsor

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Approved 16 November 1999

American National Standards Institute

Abstract: The information content and the data formats for the interchange of digital test program data between digital automated test program generators (DATPGs) and automatic test equipment (ATE) for board-level printed circuit assemblies are defined. This information can be broadly grouped into data that defines the following: UUT Model, Stimulus and Response, Fault Dictionary, and Probe.

Keywords: automatic test equipment (ATE), digital automated test program generator (DATPG), digital test interchange format (DTIF), Fault Dictionary data

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IEEE Introduction

[This introduction is not part of IEEE Std 1445-1998, IEEE Standard for Digital Test Interchange Format (DTIF).]

A digital automated test program generator (DATPG) produces test pattern and diagnostic data that can be used for testing printed circuit assemblies on automatic test equipment (ATE). The use of several DATPGs, all with individual output formats, created a need for many unique post-processors to be developed and maintained for the life of the ATE. These post-processors supported the link from specific DATPGs to specific testers. The proliferation of unique formats and post-processors created logistical support problems and therefore identified a need for standardization. A DATPG and ATE independent output data format is required to limit the number of post-processors (one for each ATE) requiring life cycle support. The digital test interchange format (DTIF) was chosen because of its wide use and because it was becoming known in industry as the de facto standard.

This document provides the basis to standardize digital test information for use on ATE. The digital test information consists of the unit under test (UUT) Model information, Stimulus and Response data, Fault Dictionary data, and Probe data.

DTIF is unique from other standards such as IEEE P1450 (Draft 0.95, dated July 1998),[1] Draft Standard Test Interface Language (STIL) for Digital Test Vector Data, and IEEE Std 1029.1-1991, IEEE Standard for Waveform and Vector Exchange Specification (WAVES). STIL is being developed to standardize the output interface of existing computer-aided engineering (CAE) tools with the input interface of ATE for integrated circuit (IC) testing only. WAVES is a hardware descriptive language used for defining stimulus and response, and their associated timing for IC/board-level design. Neither STIL nor WAVES provides for board-level fault diagnostics.

A future revision of this standard will consider the use of the information model.

1 IEEE P1450 is an IEEE authorized standards project that was not approved by the IEEE-SA Standards Board at the time this publication went to press. For information about obtaining the draft, contact the IEEE.

Digital Test Interchange Format (DTIF)

1. Overview

The digital test interchange format (DTIF) is designed to provide a mechanism for digital test data interchange independent of specific digital automated test program generators (DATPGs) and test systems. The DTIF provides a neutral database for the development and delivery of digital simulation based test program sets (TPSs). DTIF functionally supports the unit under test (UUT) Model, Stimulus and Response, Fault Dictionary, and Probe databases.

1.1 Scope

This standard defines the information content and the data formats for the interchange of digital test program data between DATPGs and automatic test equipment (ATE) for board-level printed circuit assemblies. This information can be broadly grouped into data that defines the following:

a) UUT Model;
b) Stimulus and Response;
c) Fault Dictionary;
d) Probe.

1.2 Purpose

The purpose of this standard is to provide a standard output format for test data generated by a DATPG. A DATPG produces test patterns and fault diagnostic data for ATE. This data is used in applications such as board-level assemblies where diagnostic data interchange is important.

1.3 Application

This standard is primarily intended for use by digital simulator developers/maintainers and TPS developers/maintainers.

2. References

This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

ANSI X3.4-1986 (Reaff 1997), Information Systems—Coded Character Sets—7-Bit American National Standard Code for Information Interchange (7-Bit ASCII).[1]

IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronics Terms.[2]

3. Definitions and acronyms

3.1 Definitions

The following definitions are for use with this standard. For other uses and for definitions not contained herein, see IEEE Std 100-1996. Unless otherwise indicated, the ATPG subcommittee formulated all terms defined in this subclause.

3.1.1 burst: A set of stimulus patterns and related unit under test (UUT) responses that are set up, applied, and read as a group. A test program may employ more than one burst to provide the stimuli and responses necessary to test the UUT.

3.1.2 channel: The tester electronics associated with a digital input/output (I/O) pin that either drives or senses a particular node on the unit under test (UUT).

3.1.3 circuit simulator: A software program that predicts a circuit's response to a given stimulus.

3.1.4 digital automatic test program generator (DATPG): A program, often based on simulation, that aids in the development of test patterns and diagnostic information from the model of a unit under test (UUT).

3.1.5 dynamic patterns: A set of controlled, time-variant patterns within a time interval.

3.1.6 edge: A logic state transition that is considered instantaneous for a given pattern in the simulation process.

3.1.7 end-to-end test: A test sequence to establish pass (functioning properly) or fail (not functioning properly) conditions. *Syn:* **go/nogo test.**

3.1.8 fault set: A group of one or more faults with the same fault signature.

3.1.9 fault signature: A set of unique primary output patterns in which the fault will produce a response different from the good machine response.

3.1.10 fault title: A two-part description that includes a node name and a fault type [i.e, <U5>6 SA1 (component: U5, pin: 6, fault type: Stuck at 1)].

3.1.11 go/nogo test: *See:* **end-to-end test.**

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[1]ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA (http://www.ansi.org/).

[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://www.standards.ieee.org/).

3.1.12 logic state: The representation a simulator uses to describe the state of a circuit during digital logic simulation. There are four types of logic states that exist in a typical simulator: 0, 1, Z, and X.

3.1.13 main model: The top-level unit under test (UUT) model description that includes a list of component packages and a netlist.

3.1.14 netlist: A point-to-point description of the interconnections between individual components in a circuit.

3.1.15 patterns: A set of unit under test (UUT) stimulus and expected response states. A pattern contains one unit of logic state (0, 1, X, Z) data for each UUT input and each UUT output pin.

3.1.16 phase: The time within a timing cycle when a primary input is in transition between logic states.

3.1.17 primary input (PI): A node in a circuit in which the tester can apply stimulus.

3.1.18 primary output (PO): A node in a circuit in which the tester can observe a response.

3.1.19 primary output patterns (POPAT): A set of unique responses at the node in which a fault or a group of faults are detected.

3.1.20 probe: A tester instrument used to observe the state of a node.

3.1.21 probeable node: Any node that is physically accessible to a tester probe.

3.1.22 probe window: The period of time during a pattern when a probe can capture activity on a node.

3.1.23 probing: A fault diagnostic technique that incorporates the use of a portable device (hand-held or robotic) to monitor or capture unit under test (UUT) response data. The location of the probe placement is determined by the circuit response and the circuit topology.

3.1.24 simulation time unit (STU): A fixed unit of time that is utilized during simulation for evaluation of data.

3.1.25 skew: The timing ambiguity associated with the occurrence of an automatic test equipment (ATE) Input/Output (I/O) event that is due to the physical limitations of the ATE digital driver and detector electronics.

3.1.26 static patterns: A set of controlled, time-invariant patterns.

3.1.27 stimulus: The logic states within a pattern that drives a circuit model in simulation, or a unit under test (UUT) on an automatic test equipment (ATE).

3.1.28 strobe: To record or measure the state of a particular node at an instant in time. Strobing will have a skew associated with it.

3.1.29 threshold voltage: The minimum voltage considered to be a high state or the maximum voltage considered to be a low state.

3.1.30 timing ambiguity: The period of time in a nodal transition during which the state of the node cannot be guaranteed.

3.1.31 timing generator: The function in the automatic test equipment (ATE) that stores and produces timing sets, or its analogous construct in the simulation process.

3.1.32 timing set (TSET): An automatic test equipment (ATE) timing-cycle during which stimuli are applied and unit under test (UUT) responses are measured. A timing set includes the specification of the pattern period, UUT input pin groupings that will transition at a specific time within a pattern, and UUT output pin groupings that share the same window.

3.1.33 trace: A diagnostic fault isolation program that uses a probe on a tester.

3.1.34 window: The period of time during a pattern cycle when a primary output is actively monitored by an automatic test equipment (ATE) channel.

3.2 Acronyms

ASCII	American Standards Code for Information Interchange
ATE	automatic test equipment
CAE	computer-aided engineering
DATPG	digital automated test program generator
DTIF	digital test interchange format
IC	integrated circuit
I/O	input/output
FLAP	fault set last analyzed POPAT
PI	primary input
PO	primary output
POPAT	primary output patterns
STU	simulation time unit
TP	test program
TPS	test program set
TSET	timing set
UUT	unit under test

4. Data organization overview of the DTIF standard environment

Digital circuit simulators for test, measurement, and diagnostic equipment provide an effective way to predict UUT behavior (good and bad) during test on an ATE. Results of the simulation can be used to generate the data necessary to produce a test program for the digital UUT. This standard defines the data generally available from test simulation and describes its structure for use in generating digital test programs for ATE.

Digital simulators typically provide data on the UUT Model, Stimulus and Response, Fault Dictionary, and Probe. Figure 1 shows a total of 39 American Standard Code for Information Interchange (ASCII) files, which includes a Header File and 38 data files. The Header File provides summary information and a listing of the total DTIF file set generated by a simulator for a given digital circuit. The 38 data files are organized into four functional groups. Each group portrays the functional role as it relates to UUT testing. They are

a) UUT Model Group (15 data files);
b) Stimulus and Response Group (9 data files);
c) Fault Dictionary Group (6 data files);
d) Probe Group (8 data files).

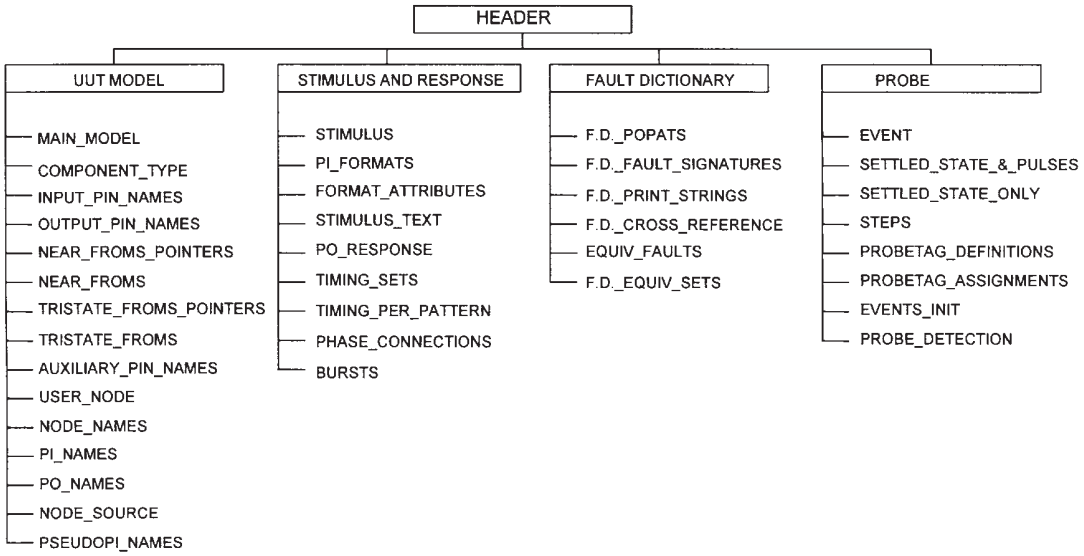

Figure 1—DTIF data files

4.1 UUT Model Group

The UUT Model Group consists of 15 data files that define the UUT Model topology. These files are used to identify the UUT/ATE interface pins, identify all the devices on the UUT, define the interconnections between devices and the structural dependencies between the inputs and outputs of a device, and to identify signal driving sources and their fan-out. They also define functional dependencies of device outputs to their inputs. The information contained in the UUT Model Group is used to develop both end-to-end and diagnostic test programs.

4.2 Stimulus and Response Group

The Stimulus and Response Group consists of 9 files. Data in these files are used to define the logic value of applied stimulus and observed good circuit response. They identify the timing of stimulus edge transitions within a pattern and the period of valid output responses within a pattern. Another function of the Stimulus and Response files is to identify groups of UUT pins with the same stimulus and response timing characteristics.

4.3 Fault Dictionary Group

The Fault Dictionary Group contains a total of 6 files. Data in these files are used on ATE to diagnose UUT failures with the fault dictionary technique. With fault dictionaries, failing responses from the UUT, captured by the ATE, are compared with the fault signatures generated in the fault simulation process and stored in ATE memory. This group identifies all faults and groups of equivalent faults, fault signatures for all detected faults, and the faults grouped within a specific fault set.

4.4 Probe Group

The Probe Group consists of a total of 8 files. They contain all the necessary information to generate probe diagnostics for an ATE. This information includes a complete history of the logic state activity and signal

timing at every device pin on the UUT, and data that assists in specifying probe window placement and timing.

5. File specifications

In this clause, the formats for each of the 39 files specified by the DTIF standard are defined. Each file consists of two or more records. One record is a line up to 80 bytes long. The records are of varying size. When writing files, trailing blanks are truncated from the records to reduce the size of the resultant file. The first record of each file shall be a Header record. All data shall be in ASCII format. The DTIF file names are not case sensitive.

All alphanumeric (character) fields are left justified. They are identified in every file description by the character 'A', and the size of each field is defined by a numeric value immediately following the character 'A.' For example, (A4) describes a four-character alphanumeric field.

All integer fields are right justified. They are identified in every file description by the character 'I,' and the size of each field is defined by an integer value immediately following the character 'I.' For example, (I6) describes a six-character integer field.

Should it be required to repeat a particular field within the file description, a multiplier may be used. For example, 5(A16) describe a sixteen-character alphanumeric field that is repeated five times.

The following pages describe the DTIF file data specifications. Each subclause includes an example specific to that file to aid in understanding. The data itself has no relationship to any other DTIF file example.