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INTERNATIONAL STANDARD

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colour
inside

Semiconductor devices – Mechanical and climatic test methods – Part 43: Guidelines for IC reliability qualification plans

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 43: Lignes directrices concernant les plans de qualification de la fiabilité des CI

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SEMICONDUCTOR DEVICES –
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FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2389/FDIS	47/2406/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This document provides guidelines for semiconductor IC vendors in the preparation of detailed reliability test plans for device qualification. Such plans are intended to be prepared before commencing qualification tests and after consultation with the user of their semiconductor integrated circuit product.

The guideline gives some examples for creating reliability qualification test plans to determine appropriate reliability test conditions based on the quality standards demanded in use conditions for each application of semiconductor integrated circuits. Categories are set for automotive applications and for general applications as a target of reliability. The grade for automotive use is further classified into two grades according to applications. The guideline assumes annual operating hours, useful life, etc. for each grade, and defines the verification methods for early failure rate and wear-out failure to propose appropriate reliability tests, and at the same time, presents concepts to properly ensure the quality of semiconductor integrated circuits using screening techniques which are designed to reduce the early failure rate.

Note that the test conditions and the values of acceleration factors presented in this guideline are shown to provide examples of calculations for obtaining reliability test conditions in order to verify the required quality standards, and are not designed to define the standards to ensure reliability of semiconductor integrated circuits.

NOTE Qualification tests are tests in which the semiconductor vendor takes account of the reliability required by its product users.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS

Part 43: Guidelines for IC reliability qualification plans

1 Scope

This part of IEC 60749 gives guidelines for reliability qualification plans of semiconductor integrated circuit products (ICs). This document is not intended for military- and space-related applications.

NOTE 1 The manufacturer can use flexible sample sizes to reduce cost and maintain reasonable reliability by this guideline adaptation based on EDR-4708, AEC Q100, JESD47 or other relevant document can also be applicable if it is specified.

NOTE 2 The Weibull distribution method used in this document is one of several methods to calculate the appropriate sample size and test conditions of a given reliability project.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-5, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-15, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-20, *Semiconductor devices – Mechanical and climatic test methods – Part 20: Resistance of plastic encapsulated SMDs to the combined effect of moisture and soldering heat*

IEC 60749-21, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-23, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-25, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-26, *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

IEC 60749-28, *Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – Device level*

IEC 60749-29, *Semiconductor devices – Mechanical and climatic test methods – Part 29: Latch-up test*

IEC 60749-42, *Semiconductor devices – Mechanical and climatic test methods – Part 42: Temperature and humidity storage*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

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- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
failure mode
style classification of a fault phenomenon which causes product failure

Note 1 to entry: Disconnection, a short circuit, occasional loss, abrasion, characteristic deterioration, etc. are typical items considered as failure modes.

3.2
failure mechanism
physical, chemical or other process which has led to a failure

3.3
integrated circuit
IC
microcircuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purpose of construction and commerce

4 Product categories and applications

Quality-related requirements, operating hours, and operating condition of ICs demanded in the field depend on the applications of products in which they are used. As an example of creating scientific test plans, their applications are broadly classified into three product categories: Automotive Use A; Automotive Use B; and Consumer Use. Table 1 shows a list of quality-related requirements according to each product category and the definition of their use conditions.

Table 1 – Examples of product categories

Category	Automotive Use A	Automotive Use B	Consumer Use
Criteria for category	Applications for automotive use directly relating to safety. (Failures can cause accidents.)	Applications for automotive use not directly relating to safety.	Applications other than for automotive use. Industrial applications shall be handled individually.
Examples of applications	Powertrains, brakes, driving support systems, airbags	Navigation systems, car air-conditioners, audio systems	Home electronics, toys, appliances
Annual operating hours	500 h (driving hours) Differs depending on whether or not to work with KEY ON/OFF.	500 h (driving hours)	Up to 8 760 h Differs among applications.
Useful life	15 years (cumulative failure probability: 0,1 %)	15 years (cumulative failure probability: 0,1 %)	Up to 10 years (cumulative failure probability: 0,1 %) Differs among applications.
Assumed operating conditions (examples of conditions which differ among applications)	**Example of engine compartment** $T_{a,min}$ = –40 °C/ $T_{a,max}$ = 125 °C $T_{j,typ}$ = 100 °C/ $T_{j,max}$ = 150 °C min. RH: 0 / max. RH: 100 %, RH (during 10 % driving) (during 70 % stop) **Example of interior environment** T_a = -40°C (min.)/85°C (max.) T_j = 85°C (typ.)/125°C (max.) RH = 0 (min.)/100 % (max.), RH (during 10 % driving) (during 70 % stop)		$T_{a,min}$ = 0 °C / $T_{a,max}$ = 70 °C T_j = 70°C/105°C (max.) RH = 10 (min.)/80 % (max.) RH (during 20 % power on) (during 60 % power off)
Early failure rate	1 × 10^{-6} or below per annum	50×10^{-6} or below per annum	Up to 500 × 10^{-6} per annum Differs among applications.
Random failure rate	10 FIT or below	50 FIT or below	>50 FIT (typical) Differs among applications.
NOTE These are examples of application conditions and requirements that do not have to all be met to be relevant for each use case.			

5 Failure

5.1 Failure distribution

Failure distribution of ICs can be broadly divided into three regions: early failure portion (e.g., t_{ELF} = 1 year), random failure portion, and wear-out failure portion. Figure 1 shows the relationship between the field use time and the instantaneous failure rate (bathtub curve). Failure distributions for each region are described in detail in 5.2 to 5.4.

Most early failures are screened within manufacturing processes of IC vendors. However, ICs not fully screened can expose problems in a relatively short period after their operation starts in the field.

Random failure has been considered to achieve a certain failure rate with respect to time, but actually, it is appropriate to consider as an extension of the early failure region where the failure rate continues to decline. Potentially induced failures outside of the supplier's control, such as ESD and EOS, should not be included in the failure rate calculations unless a total fail rate that includes these types of fail modes is intended.

Wear-out failure is a failure which occurs due to the end of life of IC components such as transistors and interconnections, and indicates the life of the ICs themselves. Wear-out failure is a failure which depends on the usage load profile (time windows may be different). The number of failures increases with time, and every IC will eventually cause a failure beyond the intended design life of the part. Wear-out failures are not considered in the same manner, because they have a totally different mechanism and therefore also a different mathematical description (failure distribution). Therefore, it is important to prevent this failure during the durable period. For ICs, the time to reach the cumulative failure probability of 0,1 % over the design life of the part in the given application is generally defined as their design lifetime.

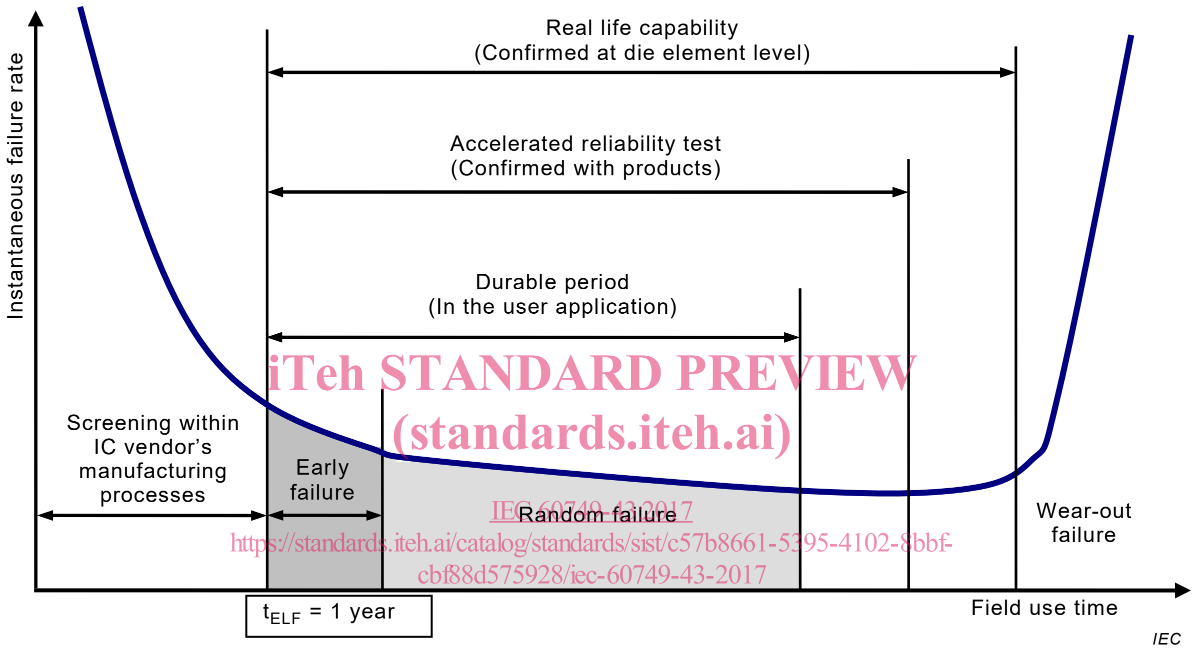

Figure 1 – Bathtub curve

5.2 Early failure

5.2.1 Description

Since ICs contain very small feature sizes and are dense and complex, they are susceptible to defects generated in manufacturing processes. For this reason, good devices which satisfy required characteristics and functions are sorted out at the final stage of manufacturing processes. The ratio of good devices to the total amount produced and tested in this process is called yield. When sorting good devices, they are measured for as many items as possible including characteristics and functions required. However, some of these sorted good devices can include those with built-in latent defects or weaknesses which does not influence electrical characteristics, and they operate properly during sorting. When the yield is high, devices with these potential defects are less likely to be included. In contrast, when the yield is relatively low, there is a high possibility of mixture of these latent defect devices with good ones. Devices with these potential defects can eventually fail during use due to the shortened lifetime or the intensity of the user application.

A small amount of tested good devices which contain such defects is included in the manufacturing lot and, as such, its failure rate decreases with time. This is because non-defective ICs which are unlikely to cause a failure remain when defective ICs are removed after they cause a failure. In such a case, the shape parameter of the Weibull distribution: m is less than 1 ($m < 1$).

To be more specific, when a manufacturing lot has good devices with a potential defect as shown in Figure 2, electronic products using such devices may cause a failure during use, and faulty ICs are removed by application screening, repair (component replacement) or disposition. This leaves reliable ICs.

NOTE It is much preferred to screen out these failures, latent or otherwise, at the IC manufacturer rather than have them reach the user, where it is more expensive to correct.

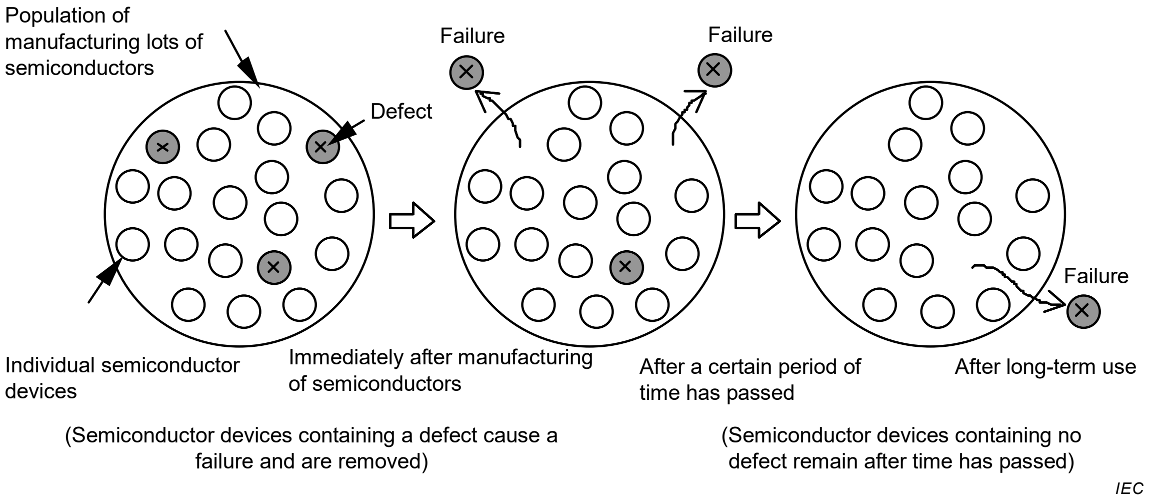

Figure 2 – Failure process of IC manufacturing lots during the early failure period

For this reason, reducing defects generated in manufacturing processes is the major countermeasure against such failures. Another possible countermeasure is to change the design to a structure not susceptible to defects if it is feasible.

There are also screening techniques such as burn-in, which operate ICs under relatively harsh conditions of temperature and/or voltage to induce the defects to fail in advance and remove them by sorting. This acts to consume the early failure period of ICs before shipment, which can reduce impacts of the early failure after shipment. Screening can be optimized if the effect of the above defect reduction is confirmed.

5.2.2 Early failure rate

5.2.2.1 Early failure rate definition

The early failure rate indicates the probability of degradation failures resulting from manufacturing defects which occur within one year (defined early failure period) after shipment by IC manufacturers and the operation starts in the field (within assembly manufacturers' processes and in end user applications).

The early failure rate is often expressed as "cumulative failure probability", where the failure rate which occurs during the defined early failure period is numerically expressed in percentage (%) or parts per million (10^{-6}).

5.2.2.2 Cumulative fail probability

In general, the cumulative failure probability is expressed as follows.

When the Weibull distribution shape parameter is expressed as m, scale parameter η and time t, the cumulative failure probability F(t): from 0 to t is defined by Formula (1).

$$F(\mathrm{t}) = 1 - \exp\left(-\frac{\mathrm{t}^m}{\eta^m}\right) \tag{1}$$

Figure 3 shows the concept of the early failure rate using a Weibull distribution chart.

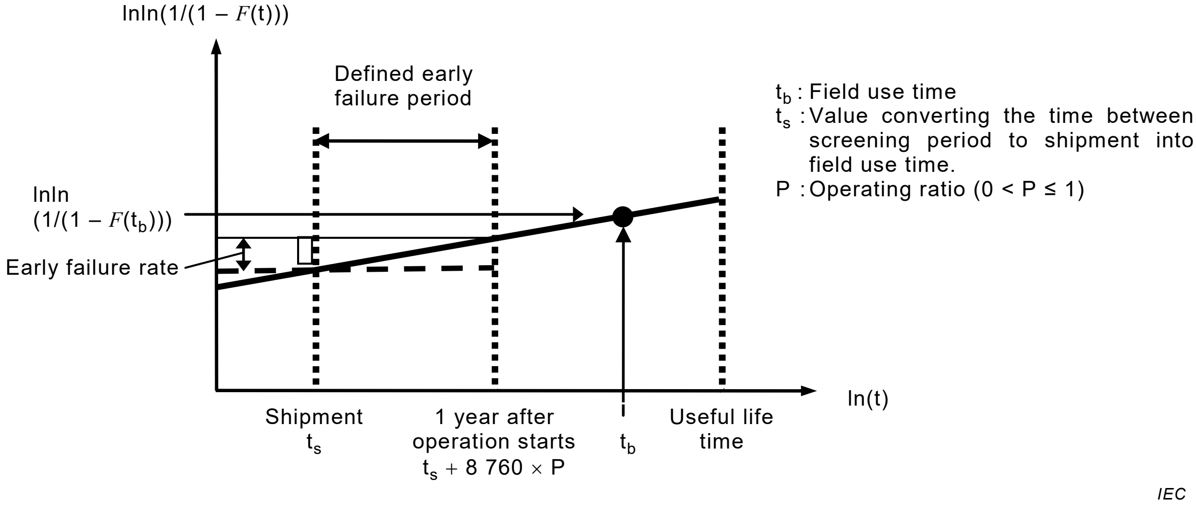

Figure 3 – Weibull conceptual diagram of the early failure rate

The following sections describe how to calculate the early failure rate from the confirmation result of the cumulative failure convergence at screening test.

5.2.2.3 Calculation of the early failure rate

Suppose that the cumulative failure probability $F(\mathrm{t_b})$ with the field use time $\mathrm{t_b}$ was obtained as the confirmation result of the cumulative failure convergence at screening test. The Weibull shape parameter η is obtained from the following formula:

$$\eta = \frac{\mathrm{t_b}}{\left[-\ln\left(1 - F(\mathrm{t_b})\right)\right]^{\frac{1}{m}}} \tag{2}$$

Where m indicates the value obtained from the experiment result or an estimated value. However, in the above formula, if there are zero failures, then $F(\mathrm{t_b}) = 0$, and the scale parameter η is undefined, as the denominator goes to 0.

For this reason, the χ^2 (chi-squared) distribution shall be used to define the cumulative failure probability $F_\mathrm{c}(\mathrm{t_b})$ taking account of the confidence level.

However, this is based on the premise that the number of samples N is sufficiently large.

NOTE Typical confidence level used in failure rate calculations for semiconductor devices is 60 %.

The cumulative failure probability at the specified confidence level and at the field use time $F_\mathrm{c}(\mathrm{t_b})$ is given by Formula (3).

$$F_\mathrm{c}(\mathrm{t_b})\Big|_\mathrm{g} = \chi^2_{\mathrm{g},\frac{\mathrm{d}}{2\times \mathrm{N}}} \tag{3}$$

Where,

χ^2 Chi-square distribution;

g Confidence level (CL in %);

d Degree of freedom = (2 × f) + 2;

f Number of failures;

N Number of samples.

Susbtituting (3) into (2) yields the scale parameter taking account of the confidence level:

$$\eta_c = \frac{t_b}{\left[-\ln\left(1 - F_c(t_b)\right)\right]^{\frac{1}{m}}} \tag{4}$$

When the value converting the screening period until shipment into field use time t_s and the calculated value η_c are used, the early failure rate taking account of the confidence level after shipment: $F_c(t_1,t_s)$ is given by the following.

If failures are found during the early failure period, η is used instead of η_c and the early failure rate takes no account of the confidence level after shipment. $F(t_1,t_s)$ is given by the following:

$$F_c(t_1,t_s) = 1 - \exp\left[-\frac{(t_1 - t_s)^m}{\eta_c^{\,m}}\right] \tag{5}$$

$$F(t_1,t_s) = 1 - \exp\left[-\frac{(t_1 - t_s)^m}{\eta^m}\right] \tag{6}$$

For both Formulae (5) and (6), $t_1 = 365 \times 24 \times P$

where

P Operating ratio ranged from 0 (always off) to 1 (always on);

t_1 Time point of 1 year after operation start measured in hours (constant on = 8 760 hours).

5.2.2.4 Calculation of a failure rate ratio

The failure rate ratio: α between the early failure rate F_c taking account of a confidence level with g (in %) and the early failure rate F taking no account of the confidence level is expressed by the following formulae:

$$F_c = \chi^2_{g,\frac{d}{2\times N}} \tag{7}$$

$$F = \frac{f}{N} \tag{8}$$

where f = Number of failures in N = Number of samples.