

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE



AMENDMENT 1  
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**Voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission – Electrical testing**

**Valves à convertisseur de source de tension (VSC) pour le transport d'énergie en courant continu à haute tension (CCHT) – Essais électriques**

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## FOREWORD

This amendment has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment.

The text of this amendment is based on the following documents:

CDV	Report on voting
22F/299/CDV	22F/316A/RVC

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

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## CONTENTS

### 3.3 Operating states

*Replace the subclause title as follows:*

#### 3.3 Operating states of converter

### 4.1.3 Sequence of test

*Delete the subclause title.*

*Add the titles of new Subclause 4.1.8 and new Clause 15 as follows:*

#### 4.1.8 Conditions to be considered in determination of type test parameters

#### 15 Tests for dynamic braking valves

### Annex A (informative) Overview of VSC topology

*Replace the annex title as follows:*

Annex A (informative) Overview of VSC converters in HVDC power transmission

*Add the titles of new Subclauses A.5.1 to A.5.4 and new Clause A.7 as follows:*

- A.5.1 General
- A.5.2 Modular multi-level converter (MMC)
- A.5.3 Cascaded two level converter (CTL)
- A.5.4 Terminology for valves of the controllable voltage source type
- A.7 Hybrid VSC valves

Annex B (informative) Fault tolerance capability

*Replace the annex title as follows:*

Annex B (informative) Valve component fault tolerance

Figure A.9 – One possible implementation of a multi-level “voltage source” VSC valve

*Replace the figure title as follows:*

Figure A.9 - The half-bridge MMC circuit

*Add, in the list of figures, the titles of new Figures A.10 to A.13 as follows:*

- Figure A.10 – The full-bridge MMC circuit
- Figure A.11 – The half-bridge CTL circuit
- Figure A.12 – Construction terms in MMC valves
- Figure A.13 – Construction terms in CTL valves

## 1 Scope

*Add, after the first paragraph, the following two paragraphs:*

The scope of this standard includes the electrical type and production tests of dynamic braking valves which may be used in some HVDC schemes for d.c. overvoltage limitation.

This standard can be used as a guide for testing of STATCOM valves.

*Add, at the end of the last sentence of the last paragraph, the words “between the purchaser and the supplier” so that the last sentence reads as follows:*

For other types of valves, the test requirements and acceptance criteria should be agreed between the purchaser and the supplier.

## 2 Normative references

*Delete from the existing list, the following references:*

IEC 60060-1:1989, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1:2006, *Insulation co-ordination – Part 1: Definitions, principles and rules*

Add to the list, the following references:

IEC 60071 (all parts), *Insulation co-ordination*

IEC 60270:2000, *High-voltage test techniques – Partial discharge measurements*

### 3.2 Power semiconductor terms

Replace the existing introductory text, terms and definitions by the following new terms and definitions:

#### 3.2.1

##### **turn-off semiconductor device**

controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

NOTE There are several types of turn-off semiconductor devices which can be used in VSC converters for HVDC. For convenience, the term IGBT is used throughout this standard to refer to the main turn-off semiconductor device. However, the standard is equally applicable to other types of turn-off semiconductor devices.

#### 3.2.2

##### **insulated gate bipolar transistor**

##### **IGBT**

turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

NOTE By applying appropriate gate to emitter voltages, the load current can be controlled, i.e. turned on and turned off.

#### 3.2.3

##### **free-wheeling diode**

##### **FWD**

power semiconductor device with diode characteristic

NOTE 1 A FWD has two terminals: an anode (A) and a cathode (K). The current through FWDs is in the opposite direction to the IGBT current.

NOTE 2 FWDs are characterized by the capability to cope with high rates of decrease of current caused by the switching behaviour of the IGBT.

#### 3.2.4

##### **IGBT-diode pair**

arrangement of IGBT and FWD connected in inverse parallel

### 3.3 Operating states

Replace the existing title, terms and definitions by the following new title, terms and definitions.

#### 3.3 Operating states of converter

##### 3.3.1

##### **blocking state**

condition of the converter, in which a turn-off signal is applied continuously to all IGBTs of the converter

NOTE Typically, the converter is in the blocking state condition after energization.

### 3.3.2

#### **de-blocked state**

condition of the converter, in which turn-on and turn-off signals are applied repetitively to IGBTs of the converter

### 3.3.3

#### **valve protective blocking**

means of protecting the valve or converter from excessive electrical stress by the emergency turn-off of all IGBTs in one or more valves

### 3.3.4

#### **voltage step level**

voltage step caused by switching of a valve or part of a valve during the de-blocked state of the converter

NOTE For valves of the controllable voltage source type, the voltage step level corresponds to the change of voltage caused by switching one submodule or cell. For valves of the switch type, the voltage step level corresponds to the change of voltage caused by switching the complete valve.

## 3.4 VSC construction terms

*Replace the existing terms and definitions by the following new terms and definitions:*

### 3.4.1

#### **VSC phase unit**

equipment used to connect the two d.c. busbars to one a.c. terminal

### 3.4.2

#### **switch type VSC valve**

arrangement of IGBT-diode pairs connected in series and arranged to be switched simultaneously as a single function unit

### 3.4.3

#### **controllable voltage source type VSC valve**

complete controllable voltage source assembly, which is generally connected between one a.c. terminal and one d.c. terminal

### 3.4.4

#### **diode valve**

semiconductor valve containing only diodes as the main semiconductor devices, which might be used in some VSC topologies

### 3.4.5

#### **dynamic braking valve**

complete controllable device assembly, which is used to control energy absorption in braking resistor

### 3.4.6

#### **valve**

VSC valve, dynamic braking valve or diode valve according to the context

### 3.4.7

#### **submodule**

part of a VSC valve comprising controllable switches and diodes connected to a half bridge or full bridge arrangement, together with their immediate auxiliaries, storage capacitor, if any, where each controllable switch consists of only one switched valve device connected in series

**3.4.8  
cell**

MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

NOTE See Figure A.13

**3.4.9  
VSC valve level**

smallest indivisible functional unit of VSC valve

NOTE For any VSC valve in which IGBTs are connected in series and operated simultaneously, one VSC valve level is one IGBT-diode pair including its auxiliaries (see Figure A.13). For MMC type without IGBT-diode pairs connected in series one valve level is one submodule together with its auxiliaries (see Figure A.12).

**3.4.10  
diode valve level**

part of a diode valve composed of a diode and associated circuits and components, if any

**3.4.11  
redundant levels**

maximum number of series connected VSC valve levels or diode valve levels in a valve that may be short-circuited externally or internally without affecting the safe operation of the valve as demonstrated by type tests, and which if and when exceeded, would require shutdown of the valve to replace the failed levels or acceptance of increased risk of failures

NOTE In valve designs such as the cascaded two level converter, which contain two or more conduction paths within each cell and have series-connected VSC valve levels in each path, redundant levels shall be counted only in one conduction path in each cell.

**3.4.12  
dynamic braking valve level**

part of a dynamic braking valve comprising a controllable switch and an associated diode, or controllable switches and diodes connected in parallel, or controllable switches and diodes connected to a half bridge arrangement, together with their immediate auxiliaries, storage capacitor, if any

**3.5.1 valve structure**

*Replace the existing definition by the following new definition:*

structural components of a valve, required in order to physically support the valve modules

**3.5.2 valve support**

*Delete the note.*

**3.5.4 valve section**

*Replace the definition by the following new definition and notes:*

electrical assembly defined for test purposes, comprising a number of valve levels and other components, which exhibits pro-rated electrical properties of a complete valve

NOTE 1 For valves of controllable voltage source type the valve section shall include cell or submodule d.c. capacitor in addition to VSC valve levels.

NOTE 2 The minimum number of VSC or diode valve levels allowed in a valve section is defined along with the requirements of each test.

**3.5.5 valve base electronics**

*Replace the definition by the following new definition.*



electronic unit, at earth potential, providing the electrical to optical conversion between the converter control system and the VSC valves

#### 4.1.3 Sequence of test

*Delete the entire subclause, including the title, text and note.*

#### 4.1.4 Test procedure

*Replace the existing sentence with the following new text:*

The tests shall be performed in accordance with IEC 60060, where applicable with due account for IEC 60071 (all parts). Partial discharge measurements shall be performed in accordance with IEC 60270.

#### 4.1.5 Ambient temperature for testing

*Replace the text of this subclause with the following sentence:*

The tests shall be performed at the prevailing ambient temperature of the test facility, unless otherwise specified.

#### 4.1.6 Frequency for testing

*Add, at the end of the subclause, the following note:*

NOTE Guidance on the worst service conditions can be found in CIGRÉ Technical Brochure No. 447.

*Add, after 4.1.7, a new subclause as follows:*

#### 4.1.8 Conditions to be considered in determination of type test parameters

Type test parameters should be determined based on the worst operating and fault conditions to which the valve can be subjected, according to system studies. Guidance on the conditions can be found in CIGRÉ Technical Brochure No. 447.

### 4.2 Atmospheric correction factor

*Insert, between the last dashed item and the last paragraph, the following new paragraph:*

Realistic worst case combinations of temperature and humidity which can occur in practice shall be used for atmospheric correction.

#### 4.4.2 Criteria applicable to valve levels

*Replace, in this entire subclause the words “short-circuited” by “short or open circuited”*

*Delete, in the last sentence of item f), the word “total”, so that the sentence reads as follows:*

If the number of such levels exceeds 3 %, then the nature of the faults and their cause shall be reviewed and additional action, if any, agreed between purchaser and supplier.

### Table 2 – Valve level faults permitted during type tests

*Replace the words “short-circuited” by “short or open circuited”.*

## 6.2 Test object

Replace in the third sentence of the first paragraph the words “VSC /diode” by “valve”.

## 6.4 Maximum continuous operating duty test

Delete in the fifth paragraph, the last sentence “The coolant temperature shall be not less ... temperatures in service” so that the paragraph now ends with “shall be representative of that used in service”.

## 6.6 Minimum d.c. voltage test

Correct in the notation for the letter symbol  $U_W$ , the word “require” to “required”.

### 7.3.1 Valve support d.c. voltage test

Replace, in the second sentence of the first paragraph, the words “in approximately 10 s” by “as fast as possible”.

Replace the existing note and the text below the note with the following new notes and text:

NOTE 1 Where possible the test voltage should be increased from 50 % to the maximum voltage level within approximately 10 s. A longer time may be used; however, this may overstress the test object.

NOTE 2 If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity the valve support may be short-circuited and earthed for a duration of several hours. The same procedure may be followed at the end of d.c. voltage test.

The valve support d.c. test voltage  $U_{tds}$  shall be determined in accordance with the following:

1 min. test

$$U_{tds} = \pm U_{dmS1} \cdot k_3 \cdot k_t$$

3 h test

$$U_{tds} = \pm U_{dmS2} \cdot k_3$$

where

$U_{dmS1}$  is the maximum of 1 s average value of voltage appearing across the valve support as determined by the insulation coordination study;

$U_{dmS2}$  is the maximum value of the d.c. component of the steady-state operating voltage appearing across the valve support;

$k_3$  is a test safety factor;

$k_3 = 1,1$ ;

$k_t$  is the atmospheric correction factor according to 4.2.

### 7.3.2 Valve support a.c. voltage test

Replace the first paragraph as follows:

To perform the test, the two main terminals of the valve shall be connected together, and the a.c. test voltage then applied between the two main terminals thus connected and earth.

Starting from a voltage not higher than 50 % of the maximum test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

*Delete in the list of notations, the second and the third symbols and their meanings i.e. " $U_{tas1}$  is the 1 min test voltage" and " $U_{tas2}$  is the 30 min test voltage".*

### 8.3.1 MVU d.c. voltage test to earth

*Replace, in the second paragraph, the words "in approximately 10 s" by "as fast as possible".*

*Add, after the second paragraph the following new note and renumber the existing note as "NOTE 2".*

NOTE 1 Where possible the test voltage should be increased from 50 % to the maximum voltage level within approximately 10 s. A longer time may be used; however, this may overstress the test object.

*Replace the last two paragraphs including the list of notations, from "Prior to the test, the MVU terminal..." to " $k_t = 1,0$  for the 3 h test." by the following new text:*

Prior to the test and before repeating the test with voltage of opposite polarity the MVU terminals may be short-circuited together and earthed for a duration of several hours. The same procedure may be followed at the end of d.c. voltage test.

The MVU d.c. test voltage  $U_{tdm}$  shall be determined in accordance with the following:

1 min. test

$$U_{tdm} = \pm U_{dmm1} \cdot k_5 \cdot k_t$$

3 h test

$$U_{tdm} = \pm U_{dmm2} \cdot k_5$$

where

$U_{dmm1}$  is the maximum of 1 s average value of voltage appearing between the high-voltage terminal of the MVU and earth;

$U_{dmm2}$  is the maximum value of the d.c. component of the steady-state operating voltage appearing between the high-voltage terminal of the MVU and earth;

$k_5$  is a test safety factor;

$k_5 = 1,1$ ;

$k_t$  is the atmospheric correction factor according to 4.2.

### 8.3.2 MVU a.c. voltage test

*Replace the fourth paragraph "During the specified 30 min. test, the level ..." by the following new text:*

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min. period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

## 9.2 Test object

*Replace the third sentence of the first paragraph with the following new sentence:*

The test valve or valve section shall be assembled with all auxiliary components except for the valve arrester if provided.

### 9.3.1 Valve a.c. – d.c. voltage test

*Replace the entire text of this subclause by the following new text:*

This test consists of a short-duration test and a long-duration test. The short-duration test reproduces the composite a.c. – d.c. voltage resulting from certain converter or system faults.

In this test, a capacitor can be used in conjunction with an a.c. test voltage source to produce a composite a.c. – d.c. voltage waveform. Depending on the converter topology, the capacitor could be an integral part of the valve, or it could be a separate item (part of the test circuit, not part of the test object).

Alternatively, a separate d.c. voltage source could be used to substitute the capacitor.

Starting from a voltage not higher than 50 % of the maximum test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For a.c. PD (partial discharge) measurement the peak value of the periodic partial discharge recorded during the last minute of the 3 h test shall be less than 200 pC, provided that the components which are sensitive to partial discharge in the valve have been separately tested. For d.c. PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

NOTE 1 Performing the valve a.c. – d.c. voltage test presents considerable practical difficulties on valves of the “controllable voltage source” type because of the high current drawn by the in-built capacitance during start-up and the slow discharge rate of the capacitor at the end of the first part of the test. For this reason, it may be necessary to modify the test procedure when testing valves of this type. Alternative test methods to be considered include the temporary substitution of a special test capacitor with reduced capacitance but the same physical size, or the pre-charging of the cell or submodule d.c. capacitor from a separate source before commencing the test.

NOTE 2 Where possible the test voltage should be increased from 50 % to the maximum voltage level within approximately 10 s. A longer time may be used; however, this overstresses the test object.

NOTE 3 If an increasing trend in the rate or magnitude of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

NOTE 4 It may be necessary to disable gate electronics or other auxiliary circuits in this test, or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

NOTE 5 In the event that it is not possible to disable gate electronics or other auxiliary circuits in this test and interference can be proven to be caused by electronics circuit then this interference may be deducted from measurement.

NOTE 6 The use of a capacitor instead of a d.c. source in the test circuit should be mutually agreed by manufacturer and purchaser as the test voltage is higher than actual value.

The valve test voltages have a sinusoidal waveshape superimposed on a d.c. level.

The valve 10 s test voltage  $U_{tv1}$  shall be determined in accordance with the following:

$$U_{tv1} = (k_{c1} \cdot U_{tac1} \cdot \sin(2\pi ft) + U_{tdc1}) \cdot k_o \cdot k_g$$

where

$U_{ac1}$  is the peak value of maximum transient a.c. component over-voltage across valve. The limiting effect of valve arrester or pole arrester can be taken into account to derive the over-voltage in service condition;

$U_{dc1}$  is the maximum transient d.c. component over-voltage across valve. The limiting effect of valve arrester or pole arrester can be taken into account to derive the over-voltage in service condition;

$k_{c1}$  is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define  $U_{ac1}$ . For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

$k_o$  is a test scaling factor according to 4.3.2;

$k_g$  is a test safety factor;

$k_g = 1,10$ ;

$f$  is the test frequency (50 Hz or 60 Hz depending on test facilities).

The valve 3 h test voltage  $U_{tv2}$  shall be determined in accordance with the following:

<https://standards.iteh.ai/collections/standards/iec-62501-2009-amd1-2014>  
<https://standards.iteh.ai/collections/standards/iec-62501-2009-amd1-2014>

$$U_{tv2} = U_{tac2} + U_{tdc2}$$

$$U_{tac2} = \frac{\sqrt{2} \cdot U_{\max\text{-cont}} \cdot \sin(2\pi ft)}{\sqrt{3}} \cdot k_{c2} \cdot k_o \cdot k_{10}$$

$$U_{tdc2} = U_{d\max} \cdot k_o \cdot k_{10}$$

where

$U_{\max\text{-cont}}$  is the maximum steady-state phase-to-phase voltage on the a.c. system or the valve side of the transformer, if a converter transformer is used in between a.c. system and converters;

$U_{d\max}$  is the maximum value of the d.c. component of the steady-state operating voltage of the d.c. system;

$k_{c2}$  is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define  $U_{tac2}$ ;

$k_o$  is a test scaling factor according to 4.3.2;

$k_{10}$  is a test safety factor;

$k_{10} = 1,10$ ;

$f$  is the test frequency (50 Hz or 60 Hz depending on test facilities).

### 9.3.2 Valve impulse tests (general)

Add, at the end of item c), the words “and consequently the impulse tests can be omitted” so that item c) reads as follows: