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TECHNICAL SPECIFICATION

Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation –
Part 1: Crystalline silicon

colour inside

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FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC TS 62804-1, which is a technical specification, has been prepared by IEC technical committee 82: Solar photovoltaic energy systems.

The text of this standard is based on the following documents:

DTS	Report on voting
82/885/DTS	82/921A/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62804 series, published under the general title *Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation,* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

This part of IEC 62804 is for testing and evaluating the durability of crystalline silicon photovoltaic modules to stresses that induce potential-induced degradation (PID). The applied stresses, mainly system voltage, manifest themselves in different degradation mechanisms depending on the module technology. A series of Technical Specifications is therefore proposed to define PID tests for different photovoltaic module technologies.

IEC TS 62804-1 defines test methods for evaluating PID in crystalline silicon PV modules.

IEC TS 62804-2 defines test methods for evaluating PID in thin-film PV modules.

Additional Technical Specifications in the series may be introduced in the future for emerging module technologies.

Voltage potential that exists between the active circuit and the grounded module surfaces can lead to module degradation by multiple mechanisms including ionic transport in the encapsulant, superstrate or substrate; hot carriers in the cell; redistribution of charges that degrade the active layer of the cell or its surfaces; failure of adhesion at interfaces, and corrosion of module components. These degradation mechanisms in crystalline silicon photovoltaic modules caused by voltage stress and promoted by high temperature and humidity have been labeled potential-induced degradation, polarization, electrolytic corrosion, and electrochemical corrosion. They are most active in wet or damp environments, and in environments prone to soiling of modules with conductive, acidic, caustic, or ionic species that lead to increased conduction on the module surfaces. In the field, modules have been observed to degrade in positive as well as negative polarity strings depending on the cell construction, module materials, and design. The testing in this Technical Specification therefore specifies the evaluation of the effects of voltage stress in both polarities for modules that may be operated in either polarity, or in the polarity defined by the manufacturer's documented specifications. Some crystalline silicon module designs undergoing system voltage bias stress have shown degradation manifested by junction failure, leading to changes in the reverse-bias breakdown characteristics and a resulting degradation in safety because of the increased potential for development of hot spots in the module. This Technical Specification describes two methods to measure the ability of a module to withstand degradation from system voltage effects that manifest in the relatively short term.

The stress-test levels in this Technical Specification have not been related to those of the natural environment. Modules types undergoing damp heat chamber testing with a 60 °C and 85 % relative humidity stress level with the temperature, humidity, and bias voltage ramped simultaneously at the start of a 96 h stress test were found resistant to PID in outdoor tests in Florida, USA. However, to improve reproducibility, test details including environmental chamber temperature and humidity ramps and tolerances have been tightened, which very significantly reduce the total stress applied and invalidate the correspondences previously found. The relevance to real outdoor stress conditions of the test contained herein using foil as the ground conductor is also not proven. Alternative levels beyond the basic stress levels in this Technical Specification are thus included.

It is known that variability in manufacturing processes can affect the susceptibility of modules to system voltage stress. Retesting of module samples by the test protocols contained herein and according to sampling plans of IEC 60410, internal quality assurance programs, or external audits will aid in verifying not only the durability of the design of the module to system voltage stress, but also the effects of variability of the materials and manufacturing processes.

PHOTOVOLTAIC (PV) MODULES – TEST METHODS FOR THE DETECTION OF POTENTIAL-INDUCED DEGRADATION –

Part 1: Crystalline silicon

1 Scope

This part of IEC 62804 defines procedures to test and evaluate the durability of crystalline silicon photovoltaic (PV) modules to the effects of short-term high-voltage stress including potential-induced degradation (PID). Two test methods are defined that do not inherently produce equivalent results. They are given as screening tests—neither test includes all the factors existing in the natural environment that can affect the PID rate. The methods describe how to achieve a constant stress level.

The testing in this Technical Specification is designed for crystalline silicon PV modules with one or two glass surfaces, silicon cells having passivating dielectric layers, for degradation mechanisms involving mobile ions influencing the electric field over the silicon semiconductor, or electronically interacting with the silicon semiconductor itself. This Technical Specification is not intended for evaluating modules with thin-film technologies, tandem, or heterostructure devices.

This Technical Specification describes methods to measure the module design's ability to withstand degradation from system voltage effects that manifest in the relatively short term. The testing in this Technical Specification does not purport to examine certain combined effects that may occur over longer periods of time in modules such as encapsulation failure, which could lead in turn to rapid moisture ingress and electrochemical corrosion. This Technical Specification does not incorporate illumination of the module that can affect the rate of degradation.

The test methods are designed to measure PID sensitivity and will give results according to the stress levels and the module grounding configuration inherent to the respective tests. Because stress method (a), testing in an environmental chamber, employs a non-condensing humidity level to serve as a conductive pathway to electrical ground, it frequently applies less stress toward the centre of the module face and the PID effect is concentrated toward the module edges as a result. Stress method (b), contacting the surfaces with a grounded conductive electrode, evaluates cell sensitivity and some effects of the component packaging materials such as glass and encapsulant resistivity, but does not differentiate the effects of some construction methods of mitigating PID, for example, the use of rear rail mounts, edge clips, and insulating frames.

The actual durability of modules to system voltage stress will depend on the environmental conditions under which they are operated. These tests are intended to assess PV module sensitivity to PID irrespective of actual stresses under operation in different climates and systems.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-78:2012, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60410, *Sampling plans and procedures for inspection by attributes*

IEC 61215:2005, *Crystalline silicon terrestrial photovoltaic (PV) modules – Design qualification and type approval*

IEC 61730-2:2004, *Photovoltaic (PV) module safety qualification – Part 2: Requirements for testing*

ISO/IEC 17025, *General requirements for the competence of testing and calibration laboratories*

3 Samples

Four representative and identical samples (two for each polarity of the system voltage that is specified or allowed in the module documentation) shall be procured for each test. Modules not explicitly requiring string connections with one terminal grounded shall be tested in both polarities. The modules for test shall be constructed with the same process and design as the model type to be evaluated—it shall contain components including cells, encapsulant, backsheet, glass, and frame made with the same manufacturing process (process tools, materials, design, and process conditions).

Modules shall be taken at random from a production batch or batches in accordance with IEC 60410. The modules shall have been manufactured from specified materials and components in accordance with the relevant drawings and process sheets and have been subjected to the manufacturer's normal inspection, quality control, and production acceptance procedures. A control module of equivalent size and design that will not be stress tested shall be additionally procured.

When submitted to another party for testing, the submitted modules shall be complete in every detail and shall be accompanied by the manufacturer's handling, mounting and connection instructions, including the maximum permissible system voltage. Markings on the module shall conform to the requirements of IEC 61215:2005, Clause 4. If the modules tested are prototypes of a new design and not from production, this fact shall be noted in the test report (see Clause 5).

The test results relate only to the module construction tested. If a module manufacturer uses several sources for PV module components, module designs, cell designs, process designs, or differing process set points and tolerances, then four modules per permutation shall be tested. Changes of the junction boxes, cables, and connectors do not indicate retest however. In cases where the cell, module, or materials process variability or tolerances are large, testing of more than two samples per polarity will be useful for improving the confidence in the results.

If the module documentation and the nameplate specify usage of the module in strings of only one voltage polarity with respect to earth ground (one terminal of the module string tied to earth ground), then the number of modules selected for test shall be halved and stressed only in that specified polarity.

If the PV module is provided with or is specified for use with a specific means for grounding, then the grounding means shall be included and considered a part of the test sample. If the PV module is provided with or is specified for use with means for mounting that could additionally influence the module grounding, then the means for mounting shall be included and considered a part of the test sample.

4 Test procedures

4.1 General

The procedures given in the following subclauses shall be performed in the order given. Any intended or unintended changes and deviations shall be recorded and reported in detail, as indicated in Clause 5 i).

There are two methods described in this Technical Specification for application of the voltage stress as follows (see Figure 1):

a) Testing in an environmental chamber, which is based on providing an electrical contact on the module surfaces with elevated relative humidity of 85 % and temperature;

b) Contacting the surface by covering it with a grounded, electrically conducting electrode in a temperature-controlled environment with a relative humidity less than 60 %.

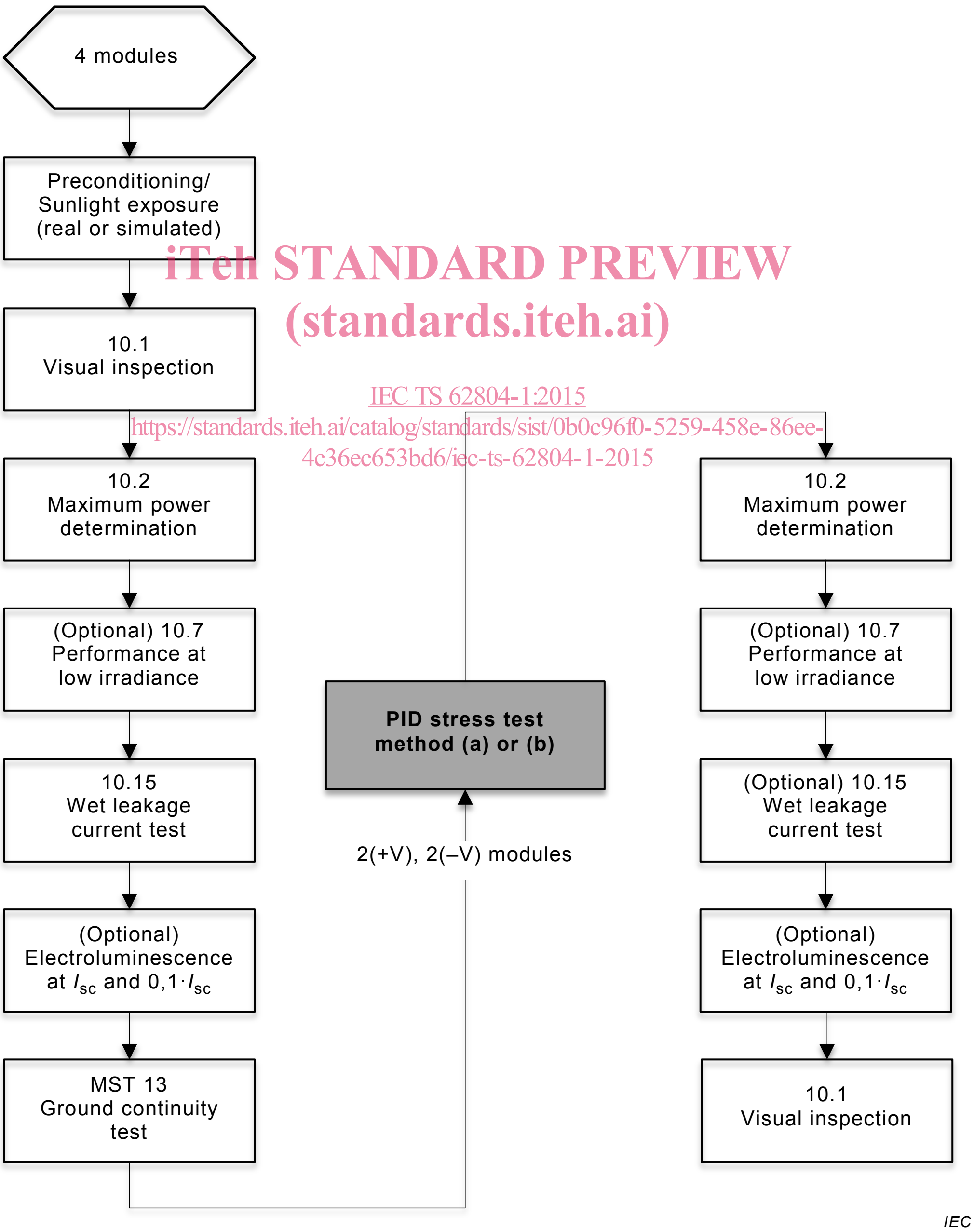

Figure 1 – PID test flow

NOTE 10.x and MST references are to clauses in IEC 61215:2005 and 61730-2:2004, respectively.

4.2 Pre-stress tests

a) All modules shall be exposed to sunlight (either real or simulated) to a target irradiation level according to the procedure for stabilization for crystalline Si modules within IEC 61215:2005, Clause 5.

b) Perform IEC 61215:2005, 10.1, Visual inspection.

c) Perform IEC 61215:2005, 10.2, Maximum power determination, including on the control module.

d) Optional: Perform IEC 61215:2005, 10.7, Performance at low irradiance, including on the control module.

NOTE 1 Loss of module power due to PID is frequently more apparent at low irradiance.

e) Perform IEC 61215:2005, 10.15, Wet leakage current test. If a wetting agent is used in the wet leakage current test, all surfaces of the modules shall be immediately and thoroughly rinsed following the wet leakage current test with water of resistivity not less than 0,05 MΩ cm that is used to generate humidity for the testing described in 4.3.2.3 (below) and according to IEC 60068-2-78:2012, 4.1. In all cases, all surfaces of the module should be wiped dry with clean cotton or paper towels and not evaporatively air-dried as the final step for the goal of avoiding sediments on the module face. This test procedure shall be terminated at this point if the module does not meet the requirements of IEC 61215:2005, 10.15, Wet leakage current test.

f) Optional: Perform electroluminescence imaging at 1 and 0,1 short circuit current (I_{sc}).

NOTE 2 Electroluminescence images are useful to identify degraded cells, which appear darker than the others.

g) Perform IEC 61730-2 MST 13, Ground continuity test, if the module has exposed conductive parts. The current for determining the resistance between conductive parts is however not specified; any current or voltage such that resistance can be evaluated may be applied.

4.3 Voltage stress test procedures

4.3.1 Apparatus

a) DC voltage power source capable of applying the maximum system voltage in the designated polarity of the modules under test with sufficient current to maintain the set-point voltage with tolerance of 0,5 % and an appropriate device for resolving and monitoring the leakage current from the module to ground.

b) Insulated wire rated for the intended test voltage, temperature, and humidity; module manufacturer-specified or stainless steel hardware for electrical connection to the modules.

c) Sensors and data logger for recording the environmental conditions (chamber air temperature, relative humidity), module temperatures to an accuracy of ±1,0 °C in a manner that demonstrates uniformity over the modules and testing space, and leakage currents (optional: applied bias voltage) of each module in 1 min or lesser intervals. Temperature sensors and their wires mounted to the module shall be electrically insulating at all applied temperatures and humidity levels so that they do not impact the voltage bias and leakage current from the module.

NOTE Current and voltage measurement and their recording are intended as indicators of stability, uniformity, and continuity of the stress test conditions and not intended as performance criteria for the module under test.

d) For procedure a) in 4.3.2, an environmental chamber capable of controlling temperature and humidity independently to achieve the stress levels for the test; non-porous, electrically insulating module support; or for procedure b) in 4.3.3, a material (e.g., aluminium or copper foil 8 μm to 150 μm in thickness) and a flexible polymeric mat to provide weighting on the foil to follow the surface morphology of the module glass to achieve a uniform electrical conducting electrode.