IEC 61189-3-719

Edition 1.0 2016-01

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Test methods for electrical materials, printed boards and other interconnection structures and assemblies –
Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling**

**Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –
Partie 3-719: Méthodes d'essai pour les structures d'interconnexion (cartes imprimées) – Contrôles de la variation de résistance des trous métallisés uniques (PTH) au cours des cycles de températures**

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CONTENTS

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling

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International Standard IEC 61189-3-719 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/1303/FDIS	91/1327/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling

1 Scope

This part of IEC 61189 specifies a test method to monitor the resistance of single plated-through holes (PTHs) in printed circuit boards (PCBs) to determine the PTH durability under thermo-mechanical stress induced by temperature cycling.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60068-2-58:2015, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IPC-2221, *Generic Standard on Printed Board Design*

3 Terms and definitions

For the purposes of this document the terms and definitions given in IEC 60194 apply, unless otherwise specified.

4 Test specimens

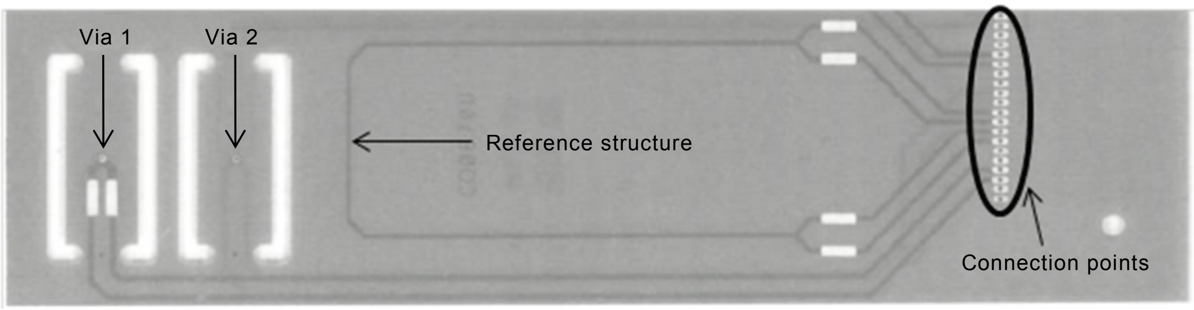
The test panels are coupons of N layer PCBs (see Figure 1 for an example of a section of a test coupon for a six-layer PCB).

If not described in the relevant specification, one test coupon shall have:

- four single through-holes connecting from the first (top, outer) to the N^{th} (bottom, outer) layer (via L1 – via LN) with the corresponding labelling;
- four single through-holes connecting from the second to the third layer (via L2 – via L3) or the (N2) to the (N1) layers with the corresponding labelling;
- one reference conductive pattern on an outer layer to compensate for possible temperature fluctuations over different temperature cycles and for resistance changes of the conductors by ageing during the test. The length of the reference structure conductive pattern is not relevant, but it is recommended to use a length similar to the length of the conductive patterns connecting the vias to the connection points (see Figure 1) and to

extend the reference structure conductive pattern over the test coupon to ensure that the reference structure is representative for the given test coupon (see Figure 1 for an example).

All structures shall feature connections to enable four wire resistance measurements. The conductive patterns shall have a cross section that is at least two times larger than the cross section in the PTHs to restrict self-heating.



IEC

Key

From left to right: first via (via 1) is connecting from the top to the bottom layer (via L1 – via L6); the second via (via 2) is connecting between inner layers (here: via L2 – via L3); middle: reference structure; right: connection points for wires connecting the test coupon to the measurement equipment.

Figure 1 – Example photograph of a section of a test coupon for a six-layer PCB

5 Test apparatus

5.1 Reflow equipment

As long as the test conditions are fulfilled, any reflow equipment may be used. The following two methods are preferred:

a) forced gas convection;

b) vapour phase.

NOTE 1 Forced gas convection is preferred, including infrared assistance.

NOTE 2 In case of vapour phase soldering, a specific vapour creating liquid is used for each test temperature.

5.2 Temperature cycling chamber

The test method uses two separate chambers or one chamber capable of cyclic temperature changes according to IEC 60068-2-14, tests Na or Nb.

5.3 Electrical resistance recording

The schematic test setup is illustrated in Figure 2. It consists of a constant direct-current source and a voltmeter. A switch can be used to subsequently measure the voltage drop at different PTHs and reference conductive patterns with the same constant-current source and voltmeter. Voltage measuring at constant current shall be performed after the panels have reached the upper cycling temperature in a temperature cycle by means of four-wire measuring and the resistance shall be calculated by dividing the measured voltage drop with the known constant current.

The test current I_{meas} to be used shall be calculated as follows: the cross-sectional area of the Cu of a PTH shall be determined. To this cross-sectional area the maximum current-carrying capacity criteria for Cu conductive patterns on inner layers for the maximum temperature increase around a conductor given in the detail specification shall be applied according to IPC-2221 to determine the test current. As an alternative, the test current can be given in the detail specification. An example of test conditions is given in Clause 8.

To avoid any resistance variations induced by different degrees of self-heating of the PTHs due to variations of the duration of the test current pulse t_{meas}, the current shall be applied long enough to establish thermal equilibrium or it should always be applied for the same period of time with a precision better than 5 %. If not given in the relevant detail specification, a test-current pulse duration of 1 s shall be applied.

NOTE Use of an application-relevant test current (as obtained by adopting the maximum current-carrying criterion for the determination of the test current) at the upper temperature of the temperature cycle ensures that self-heating of the PTH, contributing to thermal fatigue, is taken into account in the test.

According to a measurement system analysis, the setup shall have a measurement system capability with a resolution of ±5 μΩ.

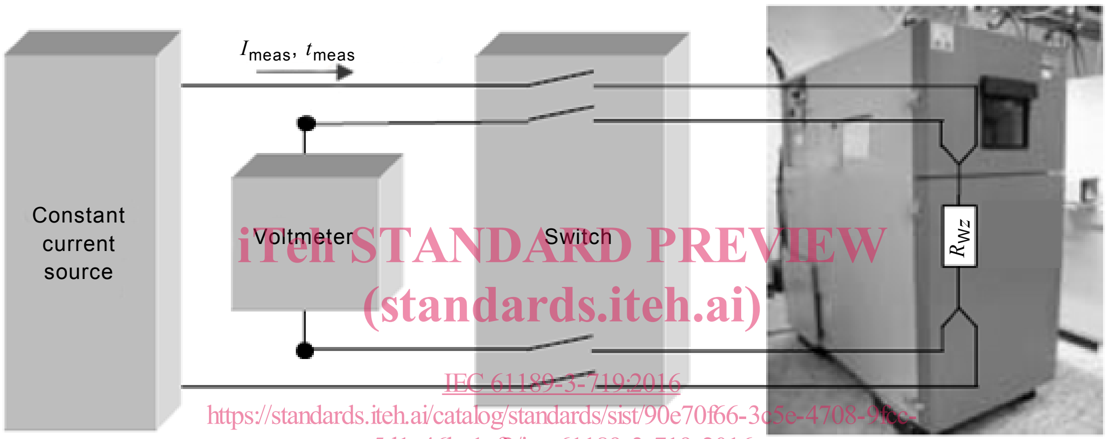


Figure 2 – Principle of online resistance measurement with high currents

6 Procedure

6.1 Preconditioning

If not detailed within the relevant specification and if the PCBs are intended for use in lead-free soldering, the PCBs shall be preconditioned by subjecting them to three reflow cycles according to the profile shown in Figure 3 and detailed in Table 1 (the minimum upper limit is specified in IEC 60068-2-58:2015, Table 7). Other preconditioning cases shall be given in the relevant specification. The temperature shall be measured on the PCB surface. This preconditioning is intended to represent the heat impact on a PCB during reflow and possibly subsequent selective soldering processes.

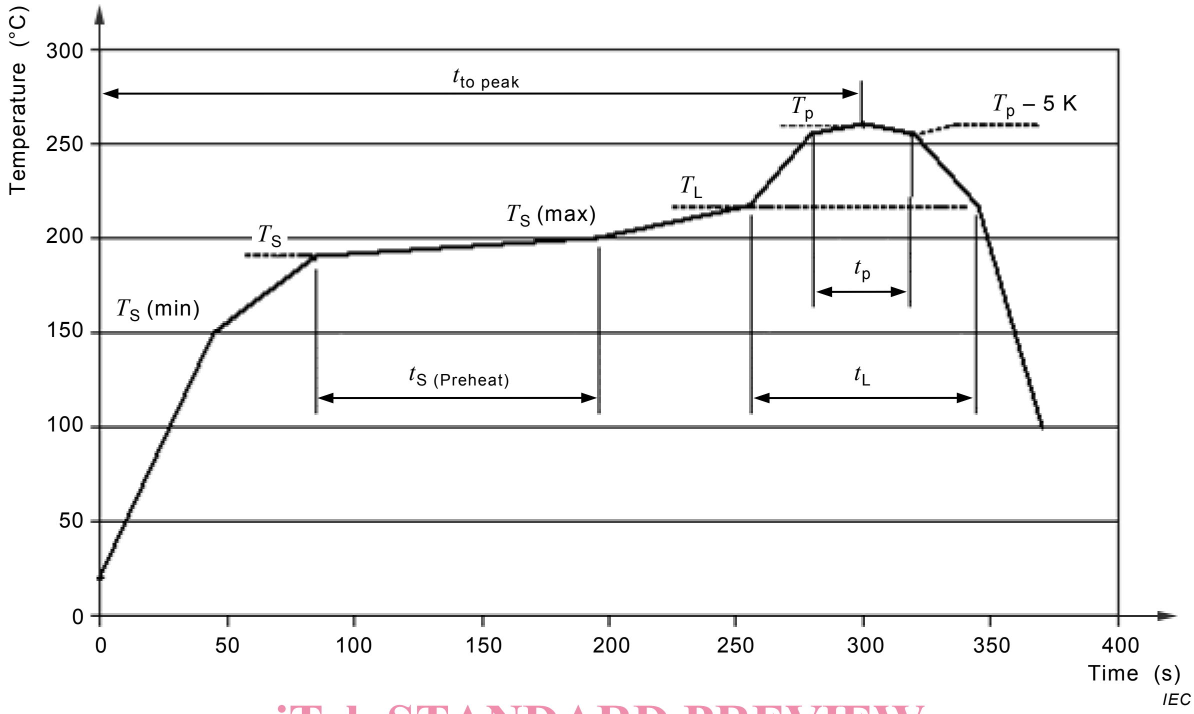


Figure 3 – Reflow temperature profile for PCB preconditioning

Table 1 – Details of the reflow temperature profile for PCB preconditioning

Preheat	
Ramp up rate 30 °C to 150 °C	min. 3 K/s (average value over 10 s)
Soak temperature (min): T_S(min)	150 °C
Soak temperature: T_S	190°C
Soak temperature (max): T_S (max)	200 °C
Soak time (T_S to T_S (max)): $t_{S(Preheat)}$	min. 110 s
Time between T_S (max) and T_L	min. 85 s
Peak	
Ramp up rate from 200 °C to T_P	min. 3 K/s (average value over 10 s)
Liquidus temperature: T_L	217 °C
Time above liquidus temperature: t_L	min. 90 s
Peak temperature: T_P	≥260 °C
Time within 5 °C of actual peak temperature: T_P – 5 K	min. 40 s
Cooling	
Ramp down rate from peak temperature	min. –6 K/s
General	
Time to peak: $t_{to\ peak}$	min. 300 s

6.2 Temperature cycling test

The printed boards shall be arranged in the temperature cycling chamber parallel to the airflow. The low temperature, T_A, and the high temperature, T_B, the duration of exposure t_1 as well as the rate of temperature change (in case of test Nb) for the temperature cycling, according to IEC 60068-2-14, tests Na or Nb, shall be given in the detail specification.

The measurement of the PTH resistances shall not take place before the working volume of the chamber and the entire PCB have reached the upper temperature in each individual temperature cycle.

Temperature variations between different measurement cycles as well as resistance changes of the conductors by ageing during the test shall be compensated by measuring of a copper reference structure on the same printed board. The temperature compensation is based on the following formulae:

Hot resistance change ΔR_z of PTH without compensation:

$$\Delta R_z = \frac{R_{\mathrm{w}z} - R_{\mathrm{w0}}}{R_{\mathrm{w0}}} \times 100\% \qquad (1)$$

Hot resistance change $\Delta R_{\mathrm{REF}z}$ of reference structure:

$$\Delta R_{\mathrm{REF}z} = \frac{R_{\mathrm{REF}z} - R_{\mathrm{REF0}}}{R_{\mathrm{REF0}}} \times 100\% \qquad (2)$$

Hot resistance change $\Delta R_{\mathrm{COMP}z}$ of PTH including temperature compensation:

$$\Delta R_{\mathrm{COMP}z} = \Delta R_z - \Delta R_{\mathrm{REF}z} \qquad (3)$$

where

$R_{\mathrm{w}z}$ is the hot resistance of PTH at cycle z in mΩ,

R_{w0} is the hot resistance of PTH at cycle 0. It is determined by the average value of the first three hot resistance values during the first three temperature cycles in mΩ,

$R_{\mathrm{REF}z}$ is the hot resistance of reference structure at cycle z in mΩ,

R_{REF0} is the hot resistance of reference structure at cycle 0. It is determined by the average value of the first three hot resistance values during the first three temperature cycles in mΩ.

If the compensated hot resistance change $\Delta R_{\mathrm{COMP}z}$ of a PTH exceeds a threshold value given in the detail specification (e.g. 5 %), the PTH has reached its end of life (EOL) due to thermo-mechanical fatigue at temperature cycle z (EOL study). In view of the statistical relevance of the result, at least 25 PTHs shall be measured individually and independently. In addition, the individual numbers of temperature cycles after which PTHs reached their EOL can be also analysed further to arrive at a Weibull distribution.

As an alternative, a pass/fail (qualification) test with a predefined number of test cycles can be conducted. The test is passed if all PTHs did not reach their EOL at a predefined number of temperature cycles as given in the detail specification.

7 Report

The report shall include:

a) test method number and revision;

b) any deviation from this test method;

c) identification and description of specimen(s);

d) PTH size, test current used in the test and threshold value for the compensated hot resistance change of a PTH for the EOL condition;