IEC 60749-44

Edition 1.0 2016-07

INTERNATIONAL STANDARD

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Semiconductor devices – Mechanical and climatic test methods – Part 44: Neutron beam irradiated single event effect (SEE) test method for semiconductor devices

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 44: Méthode d'essai des effets d'un événement isolé (SEE) irradié par un faisceau de neutrons pour des dispositifs à semiconducteurs

IEC 60749-44:2016-07(en-fr)

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ICS 31.080.01 ISBN 978-2-8322-3541-6

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 44: Neutron beam irradiated single event effect (SEE) test method for semiconductor devices

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2303/FDIS	47/2312/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 44: Neutron beam irradiated single event effect (SEE) test method for semiconductor devices

1 Scope

This part of IEC 60749 establishes a procedure for measuring the single event effects (SEEs) on high density integrated circuit semiconductor devices including data retention capability of semiconductor devices with memory when subjected to atmospheric neutron radiation produced by cosmic rays. The single event effects sensitivity is measured while the device is irradiated in a neutron beam of known flux. This test method can be applied to any type of integrated circuit.

NOTE 1 Semiconductor devices under high voltage stress can be subject to single event effects including SEB, single event burnout and SEGR single event gate rupture, for this subject which is not covered in this document, please refer to IEC 62396-4 [2].

NOTE 2 In addition to the high energy neutrons some devices can have a soft error rate due to low energy (<1 eV) thermal neutrons. For this subject which is not covered in this document, please refer to IEC 62396-5 [3].

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

None.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
critical charge
Qcrit
smallest charge that will cause a SEE if injected or deposited in the sensitive volume

3.2
single-event upset
SEU
in a semiconductor device when the radiation absorbed by the device is sufficient to change a cell's logic state

Note 1 to entry: After a new write cycle, the original state can be recovered.

3.3
multiple bit upset
MBU
energy deposited in the silicon of an electronic component by a single ionising particle causing more than one bit in the same word to be upset

Note 1 to entry: The definition of MBU has been updated due to the introduction of the definition of MCU.

3.4
multiple cell upset
MCU
energy deposited in the silicon of an electronic component by a single ionising particle inducinges several bits in an integrated circuit (IC) to be upset at one time

3.5
soft error
erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell

Note 1 to entry: As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.

Note 2 to entry: Soft errors can be generated from SEU, SEFI, MBU, MCU, and or SET. The term SER has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space and military electronics communities.

Note 3 to entry: The term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).

3.6
single event effect
SEE
response of a component caused by the impact of a single energetic particle

Note 1 to entry: Examples of energetic particle include galactic cosmic rays, solar energetic particles, energetic neutrons and protons

Note 2 to entry: The range of responses can include both non-destructive (for example upset) and destructive (for example latch-up or gate rupture) phenomena.

3.7
single-event hard error
SHE
single event induced hard error
irreversible change in operation from a single radiation event that is typically associated with permanent damage to one or more of the device elements

Note 1 to entry: Examples include permanently stuck-bit in the device and gate oxide rupture.

3.8
soft error, power cycle
PCSE
soft error that is not corrected by repeated reading or writing but can be corrected by the removal of power

3.9
flux
<particle radiation> time rate of flow of particle energy emitted from or incident on a surface, divided by the area of that surface

Note 1 to entry: The flux is usually expressed in particles per square centimetre second (N/cm^2s) or particles per square centimetre hour (N/cm^2h).

3.10
soft error rate
SER
rate at which soft errors are occurring

3.11
failure in time
FIT
failure in 10^9 device-hours

3.12
firm fault
failure that cannot be reset other than by rebooting the system or by cycling the power to the relevant functional element

3.13
hard fault
at the aircraft function level, permanent failure of a component within an LRU

Note 1 to entry: A hard fault results in the removal of the LRU affected and the replacement of the permanently damaged component before a system/system architecture can be restored to full functionality. Such a fault can impact the value for the MTBF of the LRU repaired.

3.14
single event burnout
SEB
burnout of a powered electronic component or part thereof as a result of the energy absorption triggered by an individual radiation event

3.15
single event functional interrupt
SEFI
occurrence of an upset, usually in a complex device, such that a control path is corrupted, leading the part to cease to function properly

Note 1 to entry: Examples of a complex device include microprocessors.

Note 2 to entry: This effect has sometimes been referred to as lockup, indicating that sometimes the part can be put into a “frozen” state.

3.16
single event gate rupture
SEGR
event in the gate of a powered insulated gate component when the radiation charge absorbed by the device is sufficient to cause gate rupture, which is destructive

3.17
single event latch up
SEL
event in a four layer semiconductor device when the radiation absorbed by the device is sufficient to cause a node within the powered semiconductor device to be held in a fixed state whatever input is applied until the device is de-powered

Note 1 to entry: Such latch up can be destructive or non-destructive

3.18
single event transient
SET
momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by a single energetic particle strike

Note 1 to entry: The specific terms ASET analogue single event transient and DSET digital single event transient can be used.

3.19
analogue single event transient
ASET
spurious signal or voltage produced at the output of an analogue device by the deposition of charge by a single particle

3.20
digital single event transient
DSET
spurious digital signal or voltage, induced by the deposition of charge by a single particle that can propagate through the circuit path during one clock cycle

3.21
multiple bit upset
MBU
energy deposited in the silicon of an electronic component by a single ionising particle causing upset of more than one bit in the same word

3.22
cross section
σ
<radiation terms for particle interactions>

combination of a sensitive area and probability of an interaction depositing the critical charge for a SEE

The cross section (σ) is calculated using the following formula:

$$\sigma = N / \Phi$$

Where N, is the number of errors and Φ, the particle fluence

Note 1 to entry: The units for cross section are cm^2 per device or per bit.

3.23
multiple-cell upset
MCU
event that induces several bits to fail at one time

Note 1 to entry: MCU consists of multiple-cell error bits which are usually but not always adjacent.

3.24
single bit upset
SBU
in a semiconductor device when the radiation absorbed by the device is sufficient to change a single cell’s logic state

Note 1 to entry: After a new write cycle, the original state can be recovered.

4 Test apparatus

4.1 Measurement equipment

The equipment shall be capable of measuring the functions of the integrated circuit devices, and capable of measuring the time taken for the change of stored data or other events by the exposure to energetic particles, such as neutrons, protons and alpha radiation to take place (i.e. the generation of a soft error). Alternatively, the test equipment (memory tester, etc.) shall have the capability of counting the number of soft errors in unit time. The equipment shall be capable of identifying when hard or firm faults occur; although these events are in general less frequent, their impact is higher.

NOTE The standard IEC 60749-38 contains a non-accelerated real-time soft error test.

4.2 Radiation source

In order to perform accelerated terrestrial SER measurements, a radiation source(s) is required that is similar to the energy spectrum of terrestrial cosmic rays. This can be accomplished by a broad spectrum beam or by using multiple mono-energetic beams. The radiation beam or beams should cover the whole spectrum of atmospheric radiation taking into account the energy differences in the various beams. Special attention is to be taken with respect to the effects of scattered radiation from the beam on the test setup. Technical personnel operating the facility are to be consulted in terms of the relative flux of the forward and backward scattering distribution of the beam. They shall also be consulted on effectiveness of shielding materials for the main beam and scattered beam attenuation. The number of boards in front of the device under test (DUT) and the distance from the counter shall be recorded to be used in attenuation calculations. The results of the testing shall be due to radiation effects on the DUT and not from interaction of radiation with other components in the test. In particular, power supplies can be vulnerable to radiation-induced avalanche breakdown. Sensitive electronic circuits in the tester and any device on the DUT board (e.g., buffers or registers) can also be affected. These components are to be moved as far from the primary and scattered beam as possible or appropriate shielding is to be used. Care is to be taken that the tester and power supply are not affected by scattered radiation from the beam before conducting tests in a new facility or before conducting tests with a new tester setup (including modified shielding of the tester). To assure this, the tester is to be positioned and shielded in exactly the same way as during actual tests except for the DUT that shall be positioned outside the beam or shielded from the beam. With the beam on and the DUT shielded or otherwise not exposed to the beam, test the DUT. Tester setup verification is successful if no failures are observed. Unless otherwise specified, this tester setup verification test shall last as long as a typical test. Care shall be taken to prevent upsets from stray signals or noise in the cables to the DUT. A tester readiness check shall be performed as part of the test sequence to assure electrical noise immunity.

4.3 Test sample

Any type of integrated circuits with memory can be tested. The device parameters (capacitance of the memory cell in the DRAM, etc.) which can affect the soft error rate shall be well understood. Modern complex devices including application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA) can contain more than one type of memory. These can have very different radiation upset sensitivities. FPGA as an example will generally contain configuration memory, register (flip/flop) memory and composite SRAM memory. An ASIC for example generally contains register (flip/flop) memory and composite SRAM memory. It is important that the distinction is recognised between these elements and each of the SEE rates determined separately for each type of memory bit.

5 Procedure neutron irradiated soft error test

5.1 Surface preparation

The mould compound of the DUT does not need to be etched off because the range of neutron beam in the device is sufficiently long.

5.2 Power supply voltage

Unless otherwise required, the power supply voltage shall be the nominal operating conditions specified for the device.

In order to characterize cosmic ray sensitivity as a function of Qcrit (the minimum charge needed to upset a memory cell), lower and higher voltages are also permitted.

5.3 Ambient temperature

Unless otherwise required in any specification, the ambient temperature shall be the nominal operating conditions specified for the device.

5.4 Core cycle time

The core cycle time is dependent on the samples under test (when required, the core cycle time dependence shall be measured).

5.5 Data pattern

This is dependent on the samples under test. The structure of the data patterns shall be recorded (a checker board, all 0/1-read/write pattern, etc).

Record the impact of data patterns on the observed rates.

5.6 Number of measurement samples

Multiple samples shall be measured to take into account measurement variation. If test samples are mounted along the beam line with samples behind the first sample, the beam fluence shall be calculated at each test location allowing for beam attenuation at that sample. The maximum variation in flux between different parts in the sample shall not exceed 20 %.

5.7 Calculations for time required in the beam

Information shall be provided on how to calculate, to a specified accuracy, the amount of time required in the beam, to obtain the required neutron fluence. This will be based on beam type and beam flux. Some suitable neutron beam test facilities are included in Annex B.

6 Evaluation

6.1 Measurement and failure rate estimation

The set-up of DUTs and the measuring system are the same as for the other accelerated tests.

The effective SEU cross section σ_{eff} over the specific range of energy can be defined as follows:

$$\sigma_{eff} = \frac{N_{err}}{\Phi(E_{\min}, E_{\max})} \tag{1}$$

where

N_{err} is total number of errors counted per device;

$\Phi(E_{\min}, E_{\max}$-) is the total fluence in the energy range from $E_{\min}$ to $E_{\max}$. (neuton × cm^{-2}).

On the condition that the shape of the white neutron spectrum is close enough to the field spectrum, Soft error rate (SER) or single event effect rate (SEE rate) can be estimated by

$$SER = \sigma_{eff}\,\phi_{field}(E_{\min}, E_{\max}) \tag{2}$$

where

$\phi_{field}(E_{\min}, E_{\max})$ is the neutron flux in the field (neuton.cm^{-2}.s^{-1}).