IEC/TR 62856

Edition 1.0 2013-08

TECHNICAL REPORT

RAPPORT TECHNIQUE

colour inside

Documentation on design automation subjects – The Bird's-eye View of Design Languages (BVDL)

Documentation sur les sujets concernant l'automatisation de la conception – Langages BVDL (Bird's-eye View of Design Languages)

IEC/TR 62856:2013

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

Useful links:

IEC publications search - www.iec.ch/searchpub

The advanced search enables you to find IEC publications by a variety of criteria (reference number, text, technical committee,…).
It also gives information on projects, replaced and withdrawn publications.

Electropedia - www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 30 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary (IEV) on-line.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available on-line and also once a month by email.

Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.

A propos de la CEI

La Commission Electrotechnique Internationale (CEI) est la première organisation mondiale qui élabore et publie des Normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications CEI

Le contenu technique des publications de la CEI est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

Liens utiles:

Recherche de publications CEI - www.iec.ch/searchpub

La recherche avancée vous permet de trouver des publications CEI en utilisant différents critères (numéro de référence, texte, comité d'études,…).
Elle donne aussi des informations sur les projets et les publications remplacées ou retirées.

Electropedia - www.electropedia.org

Le premier dictionnaire en ligne au monde de termes électroniques et électriques. Il contient plus de 30 000 termes et définitions en anglais et en français, ainsi que les termes équivalents dans les langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International (VEI) en ligne.

Just Published CEI - webstore.iec.ch/justpublished

Restez informé sur les nouvelles publications de la CEI. Just Published détaille les nouvelles publications parues. Disponible en ligne et aussi une fois par mois par email.

Service Clients - webstore.iec.ch/csc

Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions contactez-nous: csc@iec.ch.

IEC/TR 62856

Edition 1.0 2013-08

TECHNICAL REPORT

RAPPORT TECHNIQUE

colour inside

Documentation on design automation subjects – The Bird's-eye View of Design Languages (BVDL)

Documentation sur les sujets concernant l'automatisation de la conception – Langages BVDL (Bird's-eye View of Design Languages)

INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

PRICE CODE
CODE PRIX S

ICS 25.040

ISBN 978-2-8322-1028-4

Warning! Make sure that you obtained this publication from an authorized distributor.
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – THE BIRD'S-EYE VIEW OF DESIGN LANGUAGES (BVDL)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

The main task of IEC technical committees is to prepare International Standards. However, a technical committee may propose the publication of a technical report when it has collected data of a different kind from that which is normally published as an International Standard, for example "state of the art".

IEC 62856, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology:

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
91/1085/DTR	91/1101/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The automation of design and manufacturing technologies in electronic industries has been evolving world-wide for over three decades with remarkable development speed. Electronic design automation (EDA) technology enables the conceptualization, implementation and validation of electronic systems, that is, transforms the ideas and objectives of the system designers into manufacturable and testable representations in a cost-effective way. It is classified into three key categories such as design methodologies, design libraries and design tools. Standardization involves computer-sensible representations throughout the overall design processes which integrate design libraries and design tools to build a design ecosystem.

In the semiconductor industry EDA technologies have been substantially contributing to the unprecedented industry growth for three decades. To emerging new product lines such as microcontroller, microprocessor, ASIC, FPGA, memories, analog and mixed-signal and System on a chip (SoC) they have been continuously providing a wide range of solutions to meet critical requirements on design productivity enhancement and design quality improvement.

The EDA technical committee (EDA-TC) was formed in JEITA in 1990 in order to take initiatives for international EDA standardization in Japan. Since then, it has been contributing design language standardization such as EDIF, VHDL, Verilog HDL, Delay and Power Calculation (DPC), System C, System Verilog and Power Format, which led to forming the new working group at which experts from the industry and academia were invited and to work with IEC TC93, IEEE DASC, Accellera, Open SystemC Initiatives (OSCI) and others. After having been active for over two decades the need was felt for a bird's-eye view of the existing tens of design languages, and to enhance or develop them in order to set the strategy towards international EDA standardization. EDA-TC initiated the project in early 2009 to develop the Bird's-eye View of Design Languages (BVDL) spreadsheet documentation. It developed the first version in March 2010, in order to have an important participation of design technology experts from the semiconductor industry and academia. It finalized the BVDL documentation combined with the spreadsheet as a JEITA technical report in March 2011.

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – THE BIRD'S-EYE VIEW OF DESIGN LANGUAGES (BVDL)

1 Scope

The BVDL originally aims to make full use of planning and decision-making on EDA standardization activities for a technical expert as well as a manager in JEITA. It facilitates the understanding of the various design languages to show their positioning and features. Also it provides easy overviews of each design language for a newcomer to the EDA standards community and/or for a designer as a user of an EDA design ecosystem. Especially for a design language developer that aims to directly join design language development and voting for standardization, it provides metrics to check for duplication among similar languages, consistency to develop the design ecosystem and future challenges for design languages.

EDA standards provide a mechanism to define common semantics for electronic design ecosystems among various design tools depicted in Figure 1. The state-of-the-art standards are classified into hardware description languages, hardware verification languages, electronic system level design languages, library formats, design constrain formats, interface formats with manufacturing and testing, design data exchange formats, data models and application procedure interfaces (API), etc. Therefore they are generally called standard design languages in a narrow sense. The semiconductor industry has been facing new design complexity barriers and is today facing unprecedented complexities brought by the convergence of product features in terms of silicon process technology, system technology, high gate count and embedded software incorporation. This new design complexity requires integrated EDA solutions and at the same time impacts design ecosystem and standard design languages as well. So a new design language development or new features enhancement to an existing design language is needed. As a result tens of design languages, which might be classified into de jure standard language, de facto standard language, forum standard language and common language used in some community, are developed, enhanced or actually used in the industries, academia and communities world-wide.

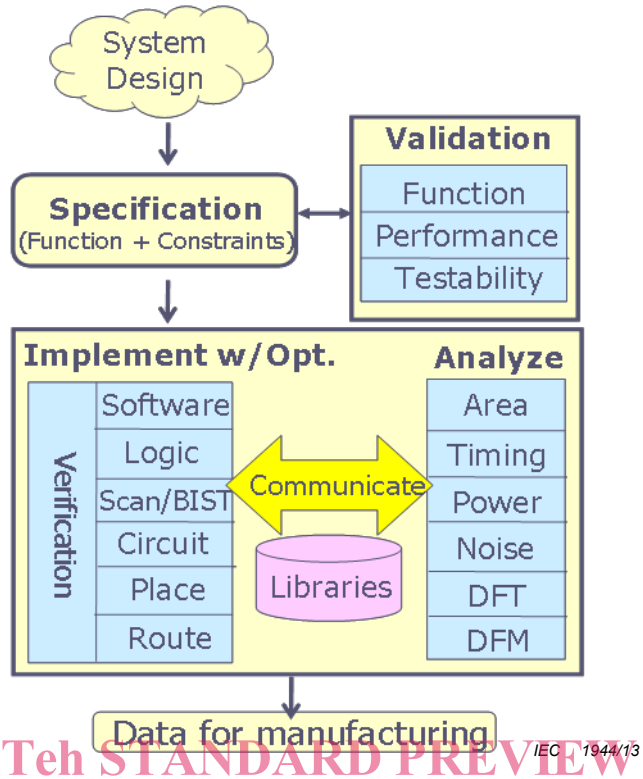


Figure 1 – Electronic design ecosystem

This technical report describes features for existing design languages, as well as for enhancing and newly developing design languages belonging to the defined design processes of System on a chip (SoC) which ranges from system level design, SoC design implementation and verification, IP block creation and analog block design down to interface data preparation for manufacturing. These simplified design processes might not become obsolete despite the remarkable speed of the evolution of electronic design automation and seem easier to understand for a non-EDA expert.

Thirty-three design languages have been chosen and each feature of their latest version as of March 2011 is reflected in this report:

UML

Esterel

Rosetta

SystemC

SystemC-AMS

IBIS

CITI

TouchStone

BSDL

System Verilog

VHDL

Verilog HDL

UPF

CPF

e language
PSL
FSDB
SDC
DEF
Open Access
SDF
GDS II
OASIS
STIL
WGL
Verilog-A
Verilog-AMS
SPICE
VHDL-AMS
LEF
Liberty
CDL
IP-XACT.

2 Structure and content of the Bird’s-eye View of Design Languages

2.1 Structure of the Bird’s-eye View of Design Languages

In 2.1, the overall structure of the Bird’s-eye View of Design Languages (BVDL) is described. BVDL consists of one chart and four tables (see Figure 2).

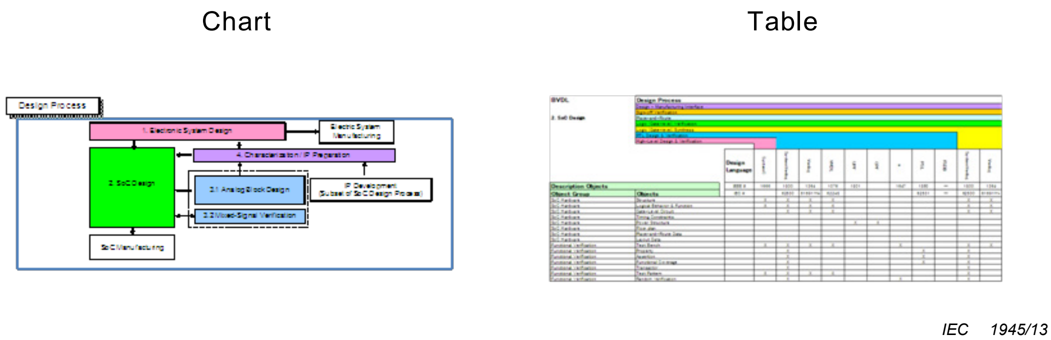
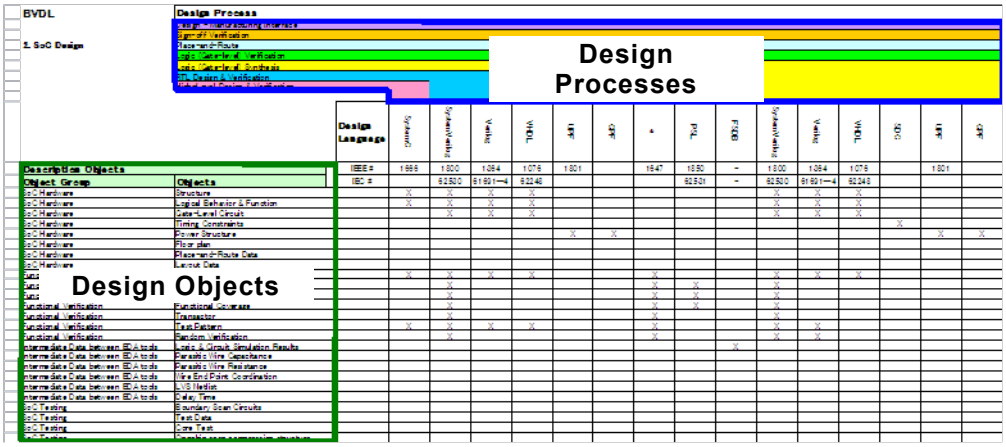


Figure 2 – Chart and table of BVDL

The purpose of BVDL is to show the positions and features of the design languages in the design processes. To help recognize them, major design processes are defined and design processes are classified into four processes such as “Electronic system design”, “SoC design”, “Mixed-signal verification and analog block design", and “Characterization and IP preparation”. The chart of BVDL shows the relations between the major design processes.

The design processes which belong to each major design process are listed in the four tables. Each table has a structure which makes it suitable to recognize the positions and features of the design languages. The design languages which are grouped according to design flow are in the columns of the tables. Design objects are in the rows of the tables. The design objects are what designers design in the design processes. For example, they are hardware description,

verification description, design constraint, and so on. They are grouped into “object groups” which represent the category. The tables have marks which show the positions and features of the languages. One language may appear in only one column or may appear in several columns (see Figure 3).

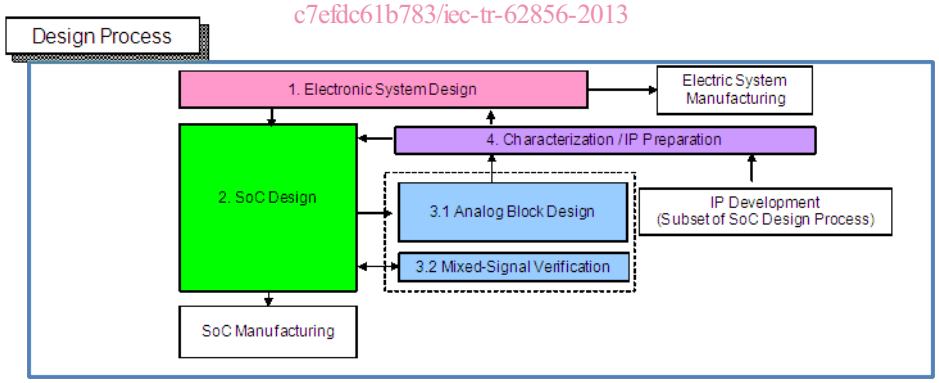


IEC 1946/13

Figure 3 – Structure of the table

2.2 Chart of design processes

In 2.2, the content of the chart of design processes is explained (see Figure 4).



IEC 1947/13

Figure 4 – Chart of design processes

In Figure 4, the four major design processes, “Electronic system design”, “SoC design”, “Mixed-signal verification and analog block design", and “Characterization and IP preparation” are defined.

The “Electronic system design” process is a design process to develop electronic systems. In the design process, system requirements are analysed and then the system specifications are defined. Printed wiring boards, packages, system architectures, and algorithms are implemented according to the specifications.

The “SoC design” process is a design process to develop Systems on a chip (SoCs). They are designed according to the specifications, system architectures, and algorithms which are

designed in the “Electronic system design” process. In the BVDL, only the digital parts of SoC designs are chosen. Although SoCs include analog circuits, the design processes of analog circuits are considered in the “Analog block design” process.

The “Analog block design” process is a design process to develop analog blocks. They are provided to the SoC design process as IPs through the “Characterization and IP preparation” process. In the “Mixed-signal verification” process, interfaces between digital parts and analog parts in SoC are verified.

In the “Characterization and IP preparation” process, digital IPs and analog IPs are prepared. These IPs are provided to the other design processes.

2.3 Table of “Electronic system design”

In 2.3, the content of the “Electronic system design” table is explained (see Figure 5).

BVDL	Design Process										
	PWB (Printed Wiring Board) Design, Package Design										
1. Electronic System Design	Architecture Design, Algorithm Design										
	Requirement Analysis, Specification Definition										
	Design Language	UML	Extend	Rosetta	SystemC	SystemC-AMS	IEIS	CITI	TouchStone	BSDL
Description Objects	IEEE #		P1778	P1699	1666		-			1149.1b
Object Group	Objects	IEC #						62014			-
Electronic System	Structure		X		X		X	X			
Electronic System	Logical Behavior & Function		X	X	X		X	X			
Electronic System	Logical Behavior & Function - Extended for AMS							X			
Electronic System	Performances & Characteristics		X		X		X	X			
Electronic System	Performances & Characteristics-Extended for AMS							X			
Electronic System	Verification Environment		X	-	X		X	X			
Electronic System	Verification Environment -Extended for AMS							X			
SoC Hardware	I/O Buffer Information								X		
SoC Testing	Boundary Scan Circuits										X
Device Characteristics	Device Characteristics (S-Parameter, etc.)								X	X	

IEC 1948/13

Figure 5 – “Electronic system design” table

The columns show the design processes in the “Electronic system design” major design process. The design processes are printed wiring board and package designs, architecture and algorithm designs, and requirement analyses and specifications definition. The design languages related to the design processes are listed in the columns.

The rows show design objects which are designed in the design processes in the columns. They are structures, logical behaviors and functions, performances and characteristics, verification environments, I/O buffer information, boundary scan circuits, and device characteristics. Their granularity should be small enough to make clear the difference between languages.

The design objects are grouped into four object groups: electronic system, SoC hardware, SoC testing, and device characteristics. The design objects, structures, logical behaviors and functions, performances and characteristics, and verification environments belong to the electronic system object group. The design object I/O buffer information belongs to the SoC hardware object group. The design object boundary scan circuits belongs to the SoC testing object group. The design object device characteristics belongs to the device characteristics object group.

2.4 Table of “SoC design”

In 2.4, the content of the “SoC design” table is explained (see Figure 6).

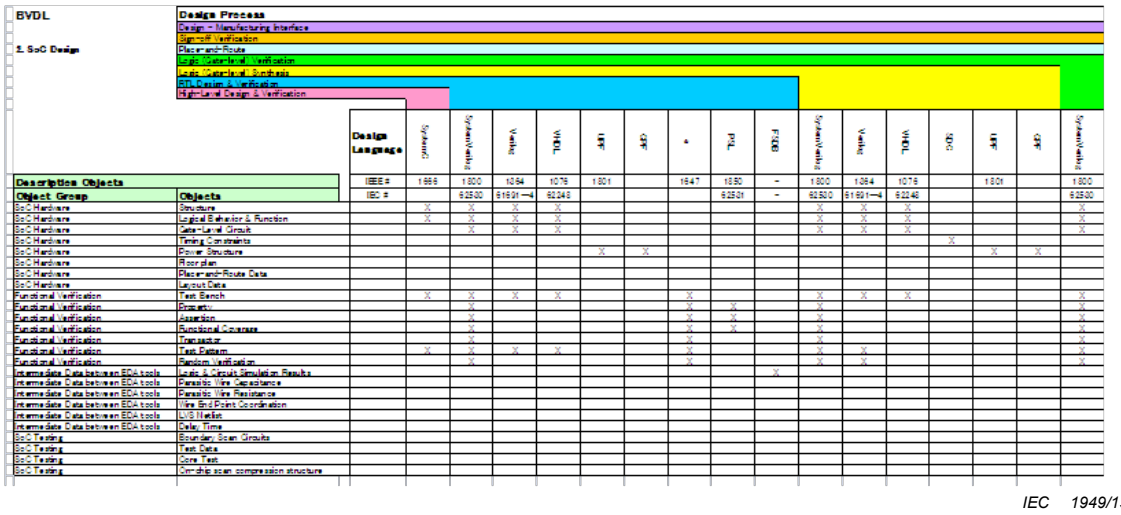


Figure 6 – Part of "SoC design" table

The columns show the design processes in the "Soc design" major design process. The design processes are high-level designs and verifications, RTL designs and verifications, logic synthesis, logic verifications, place and route, sign-off verification, and design manufacturing interface. The design languages related to the design processes are listed in the columns.

The rows show design objects which are designed in the design processes in the columns. They are structures, logical behaviors and functions, gate-level circuits, timing constraints, power structures, floor plans, place and route data, layout data, test benches, properties, assertions, functional coverage, transactors, test patterns, random verifications, logic and circuit simulation results, parasitic wire capacitance and resistance, wire end point coordinations, LVS netlist, delay time, boundary scan circuits, test data, core tests, and on-chip scan compression structures. Their granularity should be small enough to make clear the difference between languages.

The design objects are grouped into four object groups: SoC hardware, functional verification, intermediate data between EDA tools, and SoC testing. In each object group, the design objects are as follows:

In the SoC hardware object group: structures, logical behaviors and functions, gate-level circuits, timing constraints, power structures, floor plans, place-and-route data, and layout data; in the functional verification object group: test benches, properties, assertions, functional coverage, transactors, test patterns, and random verifications; in the intermediate data between EDA tools object group: logic and circuit simulation results, parasitic wire capacitances and resistances, wire end point coordinations, LVS netlists, and delay time; and in the SoC testing object group: boundary scan circuits, test data, core tests, and on-chip scan compression structures.

2.5 Table of "Mixed-signal verification" and analog block design"

In 2.5, the content of the "Mixed-signal verification and analog block design" is explained (see Figure 7).