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Information technology — Telecommunications and information exchange between systems — Synchronization methods and technical requirements for Private Integrated Services Networks

Technologies de l'information — Télécommunications et échange d'information entre systèmes — Méthodes de synchronisation et exigences techniques pour les réseaux privés avec intégration de services

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Contents

Foreword

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International Standard ISO/IEC 11573 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology,* Subcommittee SC 6, *Telecommunications and information exchange between systems*.

During the preparation of this International Standard, information was gathered on patents upon which application of the standard might depend. Relevant patents were identified as belonging to ALCATEL Business Systems. However, ISO and IEC cannot give authoritative or comprehensive information about evidence, validity or scope of patent and like rights. The patent-holder has stated that licences will be granted under reasonable terms and conditions and communications on this subject should be addressed to

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Introduction

When synchronous digital signals are being transported over a communications link, the receiving end must operate at the same average frequency as the transmitting end to prevent loss of information. This is referred to as link synchronization. When digital signals traverse a network of digital communications links, switching nodes, multiplexers, and transmission interfaces, the task of keeping all the entities operating at the same average frequency is referred to as network synchronization.

The design of a PISN requires specification of the timing sources and receivers for the synchronization network. Proper design requires that timing loops in the synchronization network be avoided. A timing loop occurs when a clock is using as its reference frequency a signal that is itself traceable to the output of that clock. The formation of such a closed timing loop leads to frequency instability and is not permitted. While it is relatively straightforward to ensure against timing loops in the primary synchronization reference network, care should be taken that timing loops do not occur during failure or error conditions when various timing references are rearranged.

When a PISN is not connected to the public digital network, synchronization can be achieved by having all PISN equipment derive timing from a single source.This source should be the highest quality clock available. Alternatively, if timing is derived from more than one class I clock, or public clock traceable source, the network is said to be operating *plesiochronously*.

If a PISN is connected to the public network at one or more nodes, the private network designer can coordinate with the public network provider to derive class I clock, or public clock traceable timing from the public digital network. More information is available in Annex A.

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Information technology — Telecommunications and information exchange between systems — Synchronization methods and technical requirements for Private Integrated Services Networks

Section 1 : General

1.1 Scope

This International Standard contains requirements necessary for the synchronization of PISNs. Timing within a digital private network needs to be controlled carefully to ensure that the rate of occurrence of slips between PINXs within the PISN, and the public switched networks is sufficiently low not to affect unduly the performance of voice transmissions, or the accuracy or throughput (if errored data require re–transmission) of non–voice services.

Requirements are also based upon the interconnection of digital private telecommunication networks via digital facilities in the public (switched or not) telecommunication networks.

This International Standard is one of a series of technical standards on telecommunications networks. This International Standard with its companion standards fills a recognized need in the telecommunications industry brought about by the increasing use of digital equipment and facilities in private networks. It is useful to anyone engaged in the manufacture of digital customer premises equipment (CPE) for private network applications, and to those purchasing, operating or applying digital CPE to digital facilities for Private Integrated Services Networks (PISN).

This International Standard establishes technical criteria necessary in the design of a synchronization plan for a PISN. Compliance with these requirements would be expected to result in a quality PISN synchronization design.

1.2 Definitions

For the purposes of this International Standard, the following definitions apply:

1.2.1 Accuracy

A measure of the maximum departure from the nominal clock rate over a 24 h period, made anytime in the lifetime of the clock, during a defined period of time, within the declared environmental conditions. Frequency deviation may be constrained to the specific accuracy by clock operation in the free running or hold over modes, as defined below.

1.2.2 Asynchronous signals

Signals having not the same nominal rate.

1.2.3 Clock free running mode

In such a mode, the PINX works with its own clock source which is not locked to an external reference and is not using storage techniques to maintain its accuracy.

1.2.4 Clock hold over mode

An operating condition of a clock in which it is not locked to an external reference clock, but uses storage techniques to maintain during a limited period of time its accuracy with respects to the last known reference clock.

1.2.5 Controlled Slip

It consists of the repetition or deletion of an integer number of octets caused by the elastic buffer mechanism used at the interface of a non–synchronous bit stream (a plesiochronous or asynchronous one). Slips and controlled slips shall be considered synonymous in this International Standard.

1.2.6 Jitter

Short–term non–cumulative variations of the significant instants of a digital signal from their ideal positions in time.

1.2.7 Lock range

Maximum frequency offset from the nominal, to which a given clock is able to synchronize.

1.2.8 Master

The term "master" refers to the clock source providing the timing to the PINX.

1.2.9 Maximum time interval error (MTIE)

The maximum time interval error (TIE) for all possible measurement intervals within the measurement period. Figure 1 illustrates the definition of MTIE.

1.2.10 Phase Locked Loop (PLL)

A feedback–controlled system that locks a local clock to an incoming reference clock in both frequency and phase.

1.2.11 Plesiochronous

The essential chracteristic of time–scales or signals such as their corresponding significant instants occur at nominally the same rate, any variation in rate being constrained within specified limits.

1.2.12 Primary Reference Clock

Equipment that provides a timing signal, with a long term accuracy equal or better than $\pm 10^{-11}$.

1.2.13 Pull in range

Maximum frequency offset from its own clock, to which a given clock is able to synchronize.

1.2.14 Reference Clock

Timing signal used for synchronization, without any assumption on its accuracy.

1.2.15 Slave

The term "slave" refers to the PINX receiving timing from another source.

1.2.16 Slip

Refer to controlled slip

1.2.17 Split Timing

An arrangement where equipment employs separate transmit and receive clocks on a transmission link having no particular relationship to one another.

1.2.18 Synchronous

Qualifies signals with corresponding significant instants occuring at the same mean rate; the time difference between these homologous instants is generally limited.

1.2.19 Synchronization

The process of adjusting the corresponding significant instants of signals so that a constant phase relationship exists between them.

1.2.20 Time–Interval Error (TIE)

The variation in time delay of a given timing signal with respect to an ideal timing signal over a particular time period. Figure 1 illustrates the definition of TIE.

1.2.21 Timing loop

An unstable condition in which two or more equipment clocks transfer timing to each other, forming a loop without a designated master timing source.

1.2.22 Time to repair

The time by which, with a stated probability, the link is repaired.

1.2.23 Transparent

A link or group of links is transparent if the signal carried is not re–timed from a clock associated with the link(s). The timing of a signal passing across a transparent link may however be altered due to jitter, wander, filtering, or fault conditions. Figure 2 illustrates the definition of transparent and non transparent links.

1.2.24 Wander

The long–term variations of the significant instants of a digital signal from their ideal positions in time. Long–term implies that these variations are of low frequency.

1.3 Abbreviations and acronyms

AIS :	Alarm Indication signal
BITS :	Building Integrated Timing Supply
CCITT :	International Telegraph and Telephone Consultative Committee
CPE :	Customer Premises Equipment
C0 :	Basic Rate transparent or non transparent links
C1 :	1,544 Mbits/s transparent or non transparent links
C2 :	2,048 Mbits/s transparent or non transparent links
C3 :	Non ISDN transparent or non transparent links
DCS :	Digital Cross–connect System
DSX :	Digital Signal Cross–connect
DTE :	Data Terminal Equipment
ESF :	Extended Super Frame
FM :	Frequency Modulation
GPS :	Global Positioning System
MTIE :	Maximum Time Interval Error (see figure1)
MUX :	Multiplexer
NCTE :	Network Channel Terminating Equipment
NI :	Network Interface
PISN :	Private Integrated Services Network.
PINX :	Private Integrated Services Network Exchange (PABX, Key System, ...).
ppm :	parts per million
PSTN :	Public Switched Telecommunication Network
PLL :	Phase Locked Loop
PRC :	Primary Reference Clock
PM :	Phase Modulation
SES :	Severely Errored Second
SDH :	Synchronous Digital Hierarchy
T0 :	Basic Rate Access to public ISDN
T1 :	1,544 Mbits/s Access to public ISDN
T2 :	2,048 Mbits/s Access to public ISDN
TIE :	Time Interval Error (see figure1)
UI :	Unit Interval (488 ns for T2 and C2, 648 ns for T1 and C1, 5208 ns for T0 and C0)
UTC :	Universal Coordinated Time

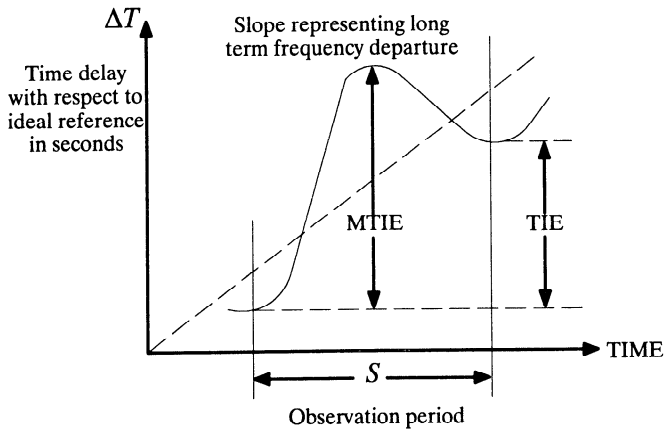


Figure 1 – Time Interval Error (TIE)

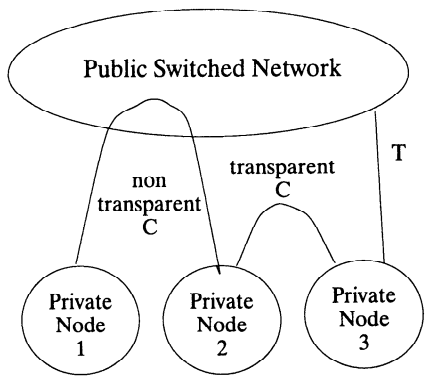


Figure 2 – Links definition

1.4 Impact of slips

When synchronous digital signals are being transported over a link, the receiving end must operate at the same average frequency as the transmitting end to prevent loss of information.

When digital signals traverse a network of digital links, switching nodes, multiplexers and transmission interfaces, the task of keeping all the entities operating at the same average frequency is referred to as synchronization. If the distant transmitter sends at a bit rate higher than the switching system clock, the receive buffer in the switching system eventually will overflow, causing one frame to be lost. If the received bit stream is at a lower bit rate, the buffer will underflow, causing a frame to be repeated. Either occurrence is called a controlled slip.

In a digital PISN, slips can be prevented by forcing all equipment to use a common reference clock. In a digital PISN, when it is not connected to the public digital network, network synchronization is achieved by having all equipments derive timing from a single source that should be the highest quality clock available.

If a PISN is connected to the public network at one or more nodes, the private network shall derive timing from the public digital network timing reference to ensure that the highest quality timing source is used.

The design of a PISN requires specification of the timing sources and receivers to achieve synchronization. Proper design requires that timing loops in the synchronization plan be eliminated.

The impact of slips on service carried on digital networks depends on the application and type of service being provided. Some examples of the effects of which are summarized in the following table.

Table 1 – Impacts of a slip

Service	Potential impact
Encrypted text	Encryption key must be retransmitted
Video	Freeze frame for several seconds Noise burst ("pop") on audio
Digital data	Deletion or repetition of data Possible misframe Reduction of throughput
Facsimile	Connection establishment may be not successful Deletion of 4–8 scan lines or lost of throughput, depending on facsimile system
Voice Band Data	Transmission errors for 0,01 to 2 s Drop call (for some modems)
Voice	Possible "Click"

In addition to slips, synchronization–related impairments caused by transmission effects on equipment such as error bursts and phase discontinuity, can also have an impact on customer service. These degradations can propagate and multiply through the network.

All of the degradations described above can be controlled by appropriate synchronization strategies and clock designs, as described in later clauses.

Section 2 : Technical requirements, Synchronization methods

2.1 Technical requirements

The phase stability of a slave clock can be described by:

– its long–term phase variations (wander and integrated frequency departure);

– its short–term phase variations (jitter);

– phase discontinuities due to transient disturbances.

NOTES

1 – The values given in 2.1.1, 2.1.2 and 2.1.3 are taken from ETS 300 012 [3] for C0 and T0, from ETS 300 011 [2] for T2 and C2 and from EIA/TIA–594 [8] for C1 and T1.

2 – It has been found necessary to limit the wander value for the T0 and C0 interfaces. The need for the additional parameters for accuracy and lock range derives from the strategies in 2.2.8.

3 – Requirements for phase discontinuity are taken from CCITT Recommendation G.812.

2.1.1 Jitter and wander at the input

2.1.1.1 C0 and T0 interfaces (144 kbits/s)

The C0 and T0 inputs shall tolerate at least a sinusoidal input jitter within the mask shown in figure 3 without producing bit errors:

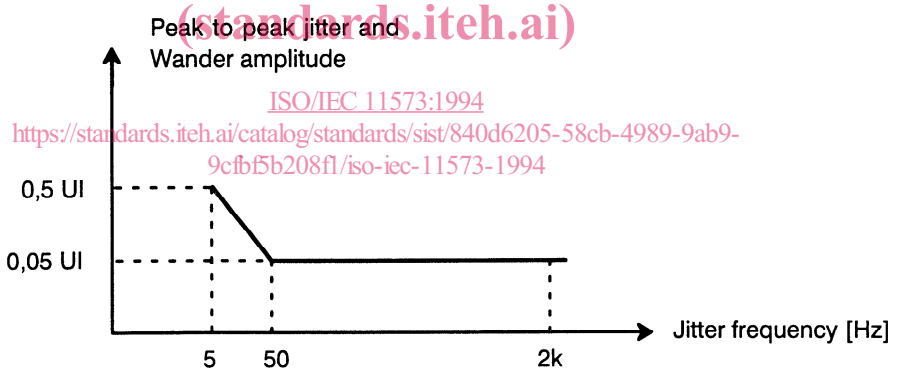


Figure 3 – Tolerable jitter and wander at PINX input for Basic Access

In order to save power, when both B channels are idle, carriers may disable T0 interfaces. Under these conditions, timing information is not available. Synchronization shall be derived from interfaces which are continuously available.

NOTE : The maximum relative wander between two or more interfaces is limited to 4 UI (except for plesiochronous operation).

2.1.1.2 C1 and T1 interfaces (1,544 Mbits/s)

The equipment shall operate with jitter of the received signal which does not exceed the following limits, in both bands simultaneously :

(1) Band 1 [10 Hz – 40 kHz] : 5,0 UI, peak–to peak, and

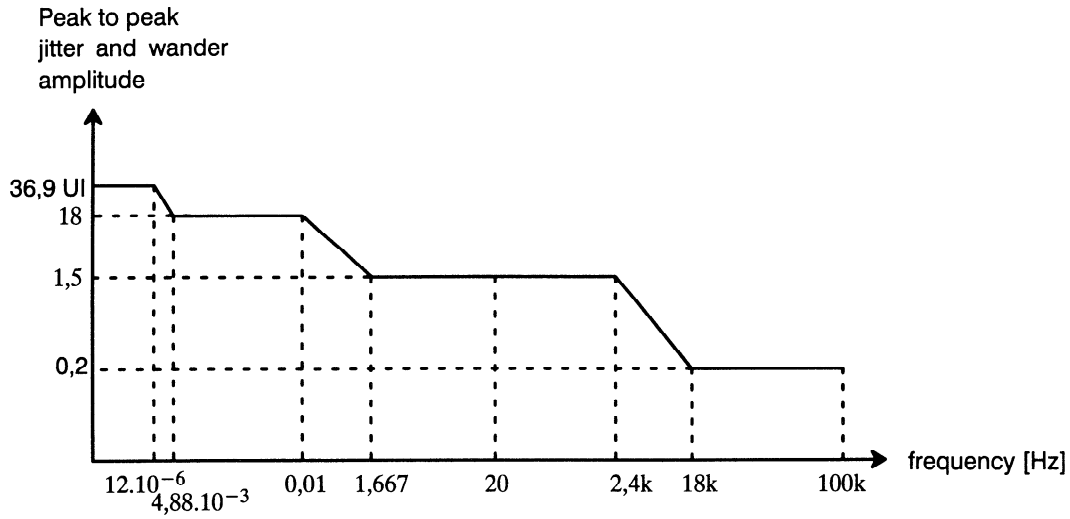
(2) Band 2 [8 kHz – 40 kHz] : 0,1 UI, peak–to–peak.

For T1 and non transparent C1 interfaces, the equipment shall operate with wander of the received signal of up to 28 UI (18 µs) peak–to–peak over any 24h period and up to 23 UI (15 µs) peak–to–peak in any 1h interval.

Wander requirements for transparent C1 interfaces are for further study.

2.1.1.3 C2 and T2 interfaces (2,048 Mbits/s)

The input shall tolerate a sinusoidal input jitter / wander within the mask shown in figure 1 without producing bit errors or losing frame alignment:



NOTE : The value of 36,9 Unit Interval (UI) is the maximum relative wander between two or more interfaces, except for plesiochronous operation.

Figure 4 – Tolerable jitter and wander at PINX input for 2Mbits/s access

2.1.2 Jitter and wander at the output

Wander accumulation within a private network needs to be controlled. Output jitter requirements of this subclause apply when the input jitter meets the requirements of 2.1.1.

2.1.2.1 C0 and T0 interfaces (144 kbits/s)

For further study.

2.1.2.2 C1 and T1 interfaces (1,544 Mbits/s)

Transmit Signal Jitter for T1 and non transparent C1 interfaces

The jitter of the transmitted signal at the equipment output interface shall not exceed the following limits, in both bands simultaneously :

(1) Band 1 0,5 UI peak–to peak, and

(2) Band 2 0,07 UI peak–to–peak.

Transmit Signal Wander for T1 and non transparent C1 interfaces

The wander in the transmitted signal of the equipment shall not exceed the wander of its received signal by more than 2,5 UI. The wander of the transmitted signal shall not exceed 28 UI (18 μs) peak–to–peak in any 24h period, nor exceed 23 UI (15 μs) peak–to–peak in any 1h interval under operating conditions defined as having class I clock, or public clock traceability over facilities with typical short–term impairments that do not include events that result in phase transients.

It is recognized that currently, the wander in the transmitted signal may be as large as 7700 UI (5 ms) peak–to–peak in any 24h period and may be as large as 4600 UI (3 ms) peak–to–peak in any 1h interval under normal operating conditions. However, it must be recognized that such wander will result in frame slips within the network.

NOTE: Transparent C1 jitter and wander requirements are for further study.

2.1.2.3 C2 and T2 interfaces (2,048 Mbits/s)

T2, one interface

band 1	f ∈ [20Hz – 100kHz]	< 1,1 UI
band 2	f ∈ [400Hz – 100kHz]	< 0,11 UI

T2, multiple interfaces and non transparent C2 interfaces

band 1	f ∈ [4Hz – 100kHz]	< 1,1 UI
band 2	f ∈ [40Hz – 100kHz]	< 0,11 UI

transparent C2 interfaces

band 1	f ∈ [4Hz – 100kHz]	< 1,6 UI
band 2	f ∈ [40Hz – 100kHz]	< 0,1 UI

2.1.3 Frequency deviation at the input

The interfaces shall tolerate input clock rates within the following ranges around the nominal value:

T0	±100 ppm
T1	±32 ppm
T2	±50 ppm

These values are only relevant for the interfaces, during maintenance and failure conditions, not for the design of the clock unit.

2.1.4 Accuracy

Accuracy is defined in 1.3

Since class I clocks are intended to be used as master clocks in plesiochronous private networks, they only operate in free running mode.

In order to conform with the strategies defined later (2.2.8), clocks shall comply with the following classes :

class I	$\leq \pm 7{,}10^{-10}$
class II	$\leq \pm 1{,}10^{-6}$
class III	$\leq \pm 50{,}10^{-6}$

NOTES:

1 In certain network configurations, clocks with higher accuracy are necessary (see Annex D).

2 Class III free running clocks are typically not used as timing sources.

2.1.5 Lock range

Slave clocks within accuracy of class II and III shall comply with one of the following lock range classes :

class a	> ±1 ppm
class b	> ±50 ppm

The following combinations of slave clocks are allowed : IIa, IIb, IIIb.

2.1.6 Phase discontinuity of slave clocks

Phase transients are changes in phase relationships. Transients are specified in terms of the maximum transient phase deviation and the maximum equivalent frequency offset during the transient. The MTIE and phase–slope requirements shall also be met under all timing reference degradations, independent of whether a switch of reference has occurred.

(1) In case of internal testing or rearrangement operations within the slave clock, the following conditions shall be met:

– the phase variation over any period of up to 2^{11} UI must not exceed 1/8 of a UI;

– for periods greater than 2^{11} UI, the phase variation for each interval of 2^{11} UI must not exceed 1/8 UI up to a total amount of 1 µs,

Where UI corresponds to the reciprocal of the bit rate of the interface.