

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Ferrite cores – Guidelines on the limits of surface irregularities –
Part 3: ETD-cores, EER-cores, EC-cores and E-cores**

**Noyaux ferrites – Lignes directrices relatives aux limites des irrégularités de
surface –
Partie 3: Noyaux ETD, EER, EC et E**

IEC 60424-3:2015

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**FERRITE CORES – GUIDELINES ON
THE LIMITS OF SURFACE IRREGULARITIES –****Part 3: ETD-cores, EER-cores, EC-cores and E-cores**

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International Standard IEC 60424-3 has been prepared IEC technical committee 51: Magnetic components and ferrite materials.

This second edition cancels and replaces the first edition published in 1999. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) addition of allowable areas of chips for EC-cores in Table 3,
- b) addition of crystallites in 4.5 and pores in 4.6.

The text of this standard is based on the following documents:

FDIS	Report on voting
51/1099/FDIS	51/1114/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60424 series, published under the general title *Ferrite cores – Guidelines on the limits of surface irregularities*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

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FERRITE CORES – GUIDELINES ON THE LIMITS OF SURFACE IRREGULARITIES –

Part 3: ETD-cores, EER-cores, EC-cores and E-cores

1 Scope

This part of IEC 60424 gives guidelines on allowable limits of surface irregularities applicable to ETD-cores, EER-cores, EC-cores and E-cores in accordance with the relevant general specification.

This standard is a specification useful in the negotiations between ferrite core manufacturers and customers about surface irregularities.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60424-1¹, *Ferrite cores – Guidelines on the limits of surface irregularities – Part 1: General specification*

IEC 60647, *Dimensions for magnetic oxide cores intended for use in power supplies (EC-cores)*

IEC 61185, *Ferrite cores (ETD-cores) intended for use in power supply applications – Dimensions*

IEC 62317-7, *Ferrite cores – Dimensions – Part 7: EER-cores*

IEC 62317-8, *Ferrite cores – Dimensions – Part 8: E-cores*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1

pore

hole left on the surface of cores after sintering and surface finishing

3.2

crystallite

grain of abnormal size distinguishable on the surface, often with sparkling facets

¹ To be published.

4 Limits of surface irregularities

4.1 Chips and ragged edges

4.1.1 General

Chips and ragged edges are defined in IEC 60424-1.

4.1.2 Chips and ragged edges on the mating surfaces

The areas of the chips located on the mating surfaces (chip1 and chip1' irregularities of Figures 1 and 2) shall not exceed the following limits:

- the cumulative area of the chips shall be less than 6 % of the mating surface (whether gapped or ungapped) of the centre leg;
- the total length of the ragged edges shall be less than 25 % of the perimeter of the relevant surface.

4.1.3 Chips and ragged edges on other surfaces

The allowable areas of chips are doubled as compared to the limits for the mating surface (see Table 1 for ETD-cores, Table 2 for EER-cores, Table 3 for EC-cores and Table 4 for E-cores).

The rule for ragged edges is the same as for the mating surface.

The allowable areas of chips for a given core are summarized in Tables 1, 2, 3 and 4.

The core sizes given in Tables 1 and 2 correspond to the cores defined in IEC 61185, IEC 62317-7, IEC 60647 and IEC 62317-8.

Table 1 – Allowable areas of chips for ETD-cores in mm²

Core size	Mating surfaces	Other surfaces
ETD19	< 2,5	< 5
ETD24	< 3,5	< 7
ETD29	< 4	< 8
ETD34	< 6	< 12,5
ETD39	< 8	< 15
ETD44	< 10	< 20
ETD49	< 12,5	< 25
ETD54	< 17,5	< 35
ETD59	< 25	< 45

Table 2 – Allowable areas of chips for EER-cores in mm²

Core size	Mating surfaces	Other surfaces
EER25,5	< 2,5	< 5
EER28	< 4	< 8
EER28L	< 4	< 8
EER35	< 6	< 12,5
EER39	< 7	< 15
EER40	< 8	< 15
EER42	< 10	< 20
EER49	< 12,5	< 25

Table 3 – Allowable areas of chips for EC-cores in mm²

Core size	Mating surfaces	Other surfaces
EC35	< 4	< 8
EC41	< 6	< 12,5
EC52	< 8	< 15
EC70	< 12,5	< 25
EC90	< 25	< 50
EC120	< 25	< 50

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Table 4 – Allowable areas of chips for E-cores in mm²

Core size	Mating surfaces	Other surfaces
E5,3/2	< 0,5	< 0,5
E6,3/2	< 0,5	< 0,5
E8/2	< 0,5	< 1
E8,3/4	< 0,5	< 1
E8,8/2	< 0,5	< 1
E10/3	< 1	< 1,5
E10,2/5	< 1	< 1,5
E13/4	< 1	< 2
E13/6	< 1	< 2
E16/4,8	< 1,5	< 3
E16/5	< 1,5	< 3
E19/5	< 1,5	< 3
E19,3/4,8	< 1,5	< 3
E20/6	< 2	< 4
E25/7	< 4	< 7
E25,4/6	< 2,5	< 5
E25,4/6,3	< 2,5	< 5
E30/11	< 7	< 14
E32/9	< 5	< 10
E33/13	< 7	< 14
E34,6/9	< 6	< 10
E35/10	< 6	< 12,5
E40/11	< 6	< 12,5
E41/13	< 10	< 20
E42/15	< 12,5	< 25
E42/20	< 15	< 30
E47/16	< 15	< 30
E50/15	< 12,5	< 25
E55/21	< 20	< 40
E55/25	< 25	< 50
E60/16	< 15	< 30
E65/27	< 30	< 60

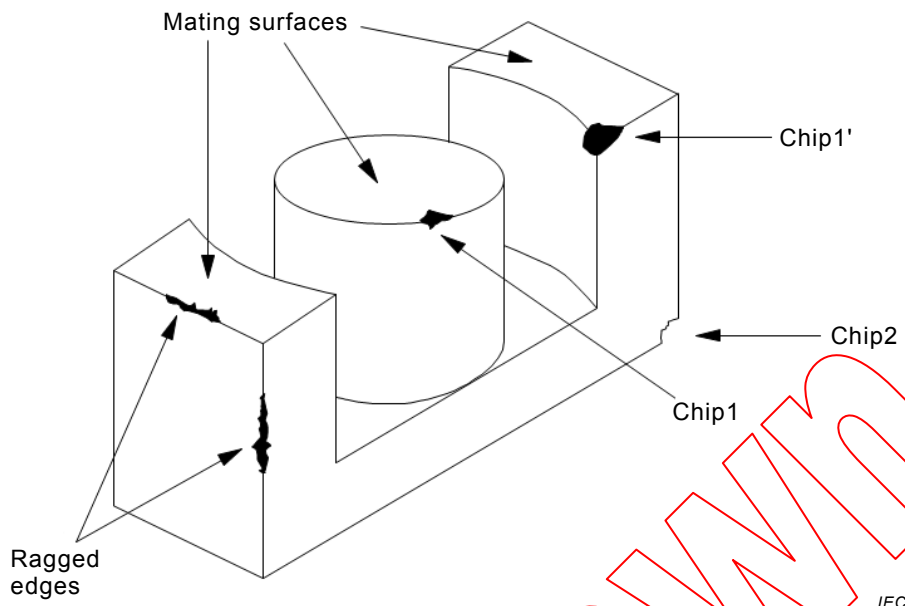


Figure 1 – Chip location for ETD-cores, EER-cores and EC-cores

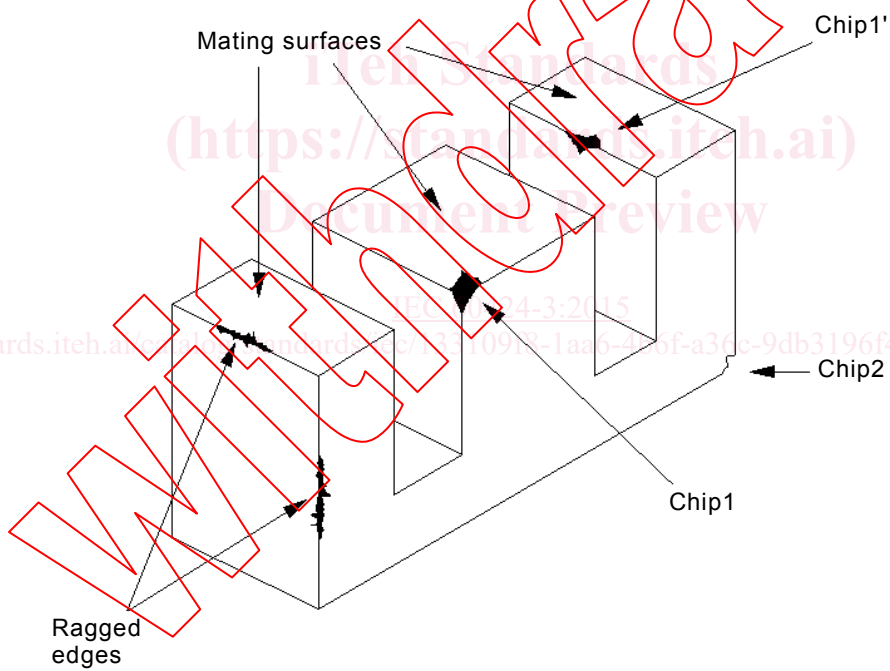


Figure 2 – Chip location for E-cores

The area and length reference for visual inspection is given in Table 5.