INTERNATIONAL STANDARD

ISO/IEC 8482

> Second edition 1993-12-15

Information technology — Telecommunications and information exchange between systems — Twisted iTeh Spair multipoint interconnections

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Technologies de l'information — Télécommunications et échange d'infor<u>mations entre sy</u>stèmes — Interconnexions multipoints par paire https://standards.it**forSedée**.g/standards/sist/e2adc014-029b-4b60-9f24-76318bf6d5f7/iso-iec-8482-1993



Foreword

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In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for vot VIEW ing. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote. (standards.iteh.ai)

International Standard ISO/IEC 8482 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*.<u>Subcommittee</u>_SC 6, *Telecommunications and information exchange between systems*.cadc014-029b-4b60-9f24-

76318bf6d5f7/iso-jec-8482-1993 This second edition cancels and replaces the first edition (ISO 8482:1987), which has been technically revised.

Annexes A and B of this International Standard are for information only.

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Information technology — Telecommunications and information exchange between systems — Twisted pair multipoint interconnections

1 Scope

1.1 This International Standard specifies the physical medium characteristics for

- twisted pair multipoint interconnections in either 2-wire or 4-wire network topology in order to provide for half duplex or duplex data transmission capability, respectively; **Teh STANDARI**

- a binary and bi-directional signal transfer of the ds.ites.athis International Standard is primarily a interconnected endpoint systems;

- the electrical and mechanical design of the endpoint <u>8482:19</u> specified for satisfactory interoperation in all possible system branch cables and the common trunk cable dards/sist configurations. Alt is the responsibility of implementors which may be up to 1 200 m in length; 76318bf6d5f7/iso-icc-840 ensure that their intended configuration will allow satisfactory interoperation.

- the component measurements of the integrated circuit type generators and receivers within the endpoint systems;

- the applicable data signalling rate up to 12,5 Mbit/s.

1.2 The defined electrical component characteristics and measurements are in close conformance with the twisted pair point-to-point characteristics given in ITU-T Recommendation V.11.

1.3 This International Standard does not describe a complete physical interface and has no functional interface characteristics, such as

- number of interchange data and control circuits;

- type, size and pin allocation of the endpoint system and branch trunk cable connectors;

- data and control signal encoding;

- time relations between signals on the interchange circuits;

- mode of synchronous or asynchronous transmission;

- signal quality for transmission and reception.

1.4 This International Standard does not specify special environmental conditions, such as galvanic isolation, electromagnetic interference (EMI), radio frequency interference (RFI), and human safety. This may form the subject of a future amendment.

1.6 This International Standard may be combined with any appropriate set of functional and additional environmental characteristics so as to meet the practical data transmission requirements in the field of local or wide area networks.

2 Normative reference

The following ITU-T Recommendation contains certain provisions which, through reference in this text, constitutes provisions of this International Standard. At the time of publication, the edition indicated was valid. All CCITT Recommendations and International Standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the recommendation indicated below. Members of IEC and ISO maintain registers of currently valid International Standards. The ITU-T Secretariat maintains а list of currently valid ITU-T Recommendations.

ITU-T Recommendation V.11:1988, *Electrical* characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications.

3 Definitions

For the purposes of this International Standard the following definitions apply:

3.1 balanced interchange circuit: An interchange circuit which uses two conductors and the differential mode voltage for transmitting signals.

3.2 common mode ejection ratio (CMRR): For balanced interchange circuits, the ratio of an applied common mode voltage, V_{cm} to the resulting transverse voltage V_{tr} (same as the differential mode voltage).

The ratio is normally expressed in decibels as

3.6 differential mode voltage: The vector difference of the voltages between each conductor of a balanced interchange circuit and ground or other stated voltage reference.

NOTE - The differential mode voltage is commonly referred to as the transverse mode voltage.

3.7 environmental conditions: Those characteristics of the electrical or physical environment, for example EMI, ground potential difference magnetic fields, altitude, temperature, etc., which may affect the operation, with respect to interchange circuits, of a DTE or DCE.

3.8 galvanic isolation: The existence of a element that is non-conductive with respect to the conductivity of common mode voltage, between the equipment containing a generator and the equipment containing a receiver of an interchange circuit.

3.9 generator: The component of an interchange circuit that is the source of the transmitted signal.

 $CM RR = 20 \log \frac{V_{cm}}{V_{tr}}$ **iTeh STANDAROTEPThe term generator** is used interchangeably with the term driver. **(standards.iteh.ai)**3.10 generator offset voltage: The d.c. component

NOTE - The rejection ratio depends upon the circuit termination and should be measured while terminated in <u>O/IEC 8489</u> of half the vector sum of the voltages between each normal use. https://standards.iteh.ai/catalog/standards/splip/2dd(114-0)/9b-4b(1)-91/4-76318bf6d5f7/iso-ieC-8482-1993

3.3 common mode voltage: One half the vector sum of the voltages between each conductor of a balanced interchange circuit and ground or other stated voltage reference.

NOTE This voltage may be a transmitted (or received) signal or noise intereference. In the latter case, this voltage is generally not the same as the voltage, which is sometimes referred to as common mode voltage, that may exist (in a common mode) between the ends of an interchange circuit pair as a result of induction or ground-reference potential difference.

3.4 cross-talk loss (near end): For two interchange circuits used for transmission in opposite directions, the ratio, expressed in decibels, of the voltage transmitted on one interchange circuit to the resulting voltage (cross-talk) at the receive end of the other interchange circuit.

3.5 cross-talk loss (far end): For two interchange circuits used for transmission in the same direction, the ratio, expressed in decibels, of the voltage transmitted on one interchange circuit to the resulting voltage (cross-talk) at the receive end on the other interchange circuit.

NOTE - The d.c. component of half the vector sum of the voltages is the same as the arithmetic mean of the d.c. voltages in the above.

3.11 ground signal: The generator/receiver signal voltage reference.

3.12 ground earth: The voltage reference established by conductive components having a conductive path to earth in the vicinity of the equipment including the generator/receiver.

NOTE - Earth ground is generally synonymous with, and the same as, frame or building ground or protective ground.

3.13 ground potential difference: The difference between the signal ground potentials of the generator and the receiver of an interchange circuit.

The potential is the same as the difference in the earth ground potential difference only if the signal ground is connected to earth ground at both the generator and the receiver.

3.14 induced noise: An interfering voltage that is ininterchange circuit an bv troduced into electromagnetic induction from currents in other conductors.

For balanced interchange circuits induced voltages generally appear in the common mode.

3.15 interchange circuit: The circuit, including a generator, a receiver and interconnecting media, that provides for the interchange of signals across an example DTE/DTE. DTE/DCE, interface. for DCE/DCE.

3.16 interchange point: The point in an interchange circuit at which the specified electrical characteristics of the circuit apply and should be measured.

NOTE - The interchange point usually defines the line of demarcation between equipment and is usually the location of an interface connector.

receiver: The component of an interchange 3.17 circuit that provides for the detection of interchange circuit signals at the receiving equipment. ANDA 3.19 site conditions: The environmental conditions for a given site.

3.20 surge voltage resistance: The ability of an interchange circuit to function normally after being subjected to surges having peak voltages up to some specified value.

NOTE - Surge voltage resistance is sometimes referred to as surge immunity.

3.21 surge voltage: A transient voltage wave appearing on an interchange circuit as a result of induction or other phenomenon and having a relatively high value and short duration.

It is normally acceptable for such surges to cause errors or malfunctions.

NOTE - Surges are normally specified with the intent of assuring that equipment will not be damaged by such unusual conditions.

3.22 unbalanced interchange circuit: An interchange circuit that uses one conductor together with a second return conductor, normally signal ground, which is used in common by several circuits.

3.18 rise time: The time required to a generator ds.i output signal voltage to change from a value characteristic of one state to a value characteristic of: 8482:1993

a second state.

It is most often specified as the time for the signal voltage to pass between the 10 % and 90 % points of the wave form.

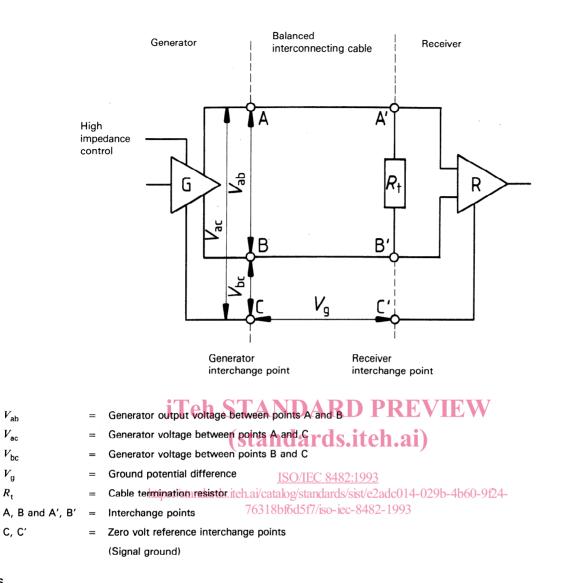
NOTES

Rise time is normally dependent on the load and is usually specified for a specific test termination.

For unbalanced generators, the time for the change from an ON or active state to an OFF or inactive state is sometimes referred to as the "fall time".

https://standards.iteh.ai/catalog/standards/sist/e2adc014-029b-4b60-9f24-76318bf6d5f7/iso-iec-8482-1993 Symbolic representation of an interchange circuit (see figure 1)

The symbolic representation of an interchange circuit is in principle as given in ITU-T Recommendation However, the generator specified in this V.11. International Standard includes an additional control to place the device into the active state or the inactive, high impedance zero voltage state. This addition is shown in the symbolic representation reproduced in figure 1.



NOTES

1 Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined without the cable termination resistor at the "receiver interchange point".

2 Points C and C' may be interconnected and further connected to protective ground if required by national regulations.

Figure 1 — Symbolic representation of interchange circuit

5 Interconnection configurations (see figures 2 and 3)

In general, the interconnection configuration consists of one balanced trunk cable, which may be up to 1 200 m in length, and several balanced branch cables, each connecting an individual endpoint system to the common trunk cable. The branch cable connection points may be spaced as appropriate. A branch cable should be kept as short as possible and in any case not exceed 1 m in length. The balanced trunk cable shall be terminated by a termination resistor at each end. This facilitates the generator/receiver load measurements defined in 6.1.2. For connection of the endpoint systems to the trunk cable, a branch/trunk cable connector should be used. The connector(s) at each end of the trunk cable shall accommodate the termination resistor(s).

Balanced cables may be shielded if required by local regulations. It may also be necessary to extend shielding across the branch/trunk cable connectors.

Depending on the type of multipoint operation, either a two wire or a four wire interconnection configuration may be used. For example, figure 2 shows a two wire multipoint configuration for half duplex data transmission, while figure 3 shows a four wire multipoint configuration for either half duplex or duplex data transmission.

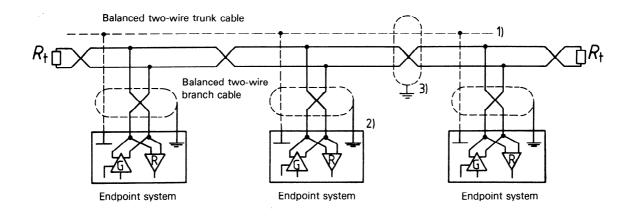
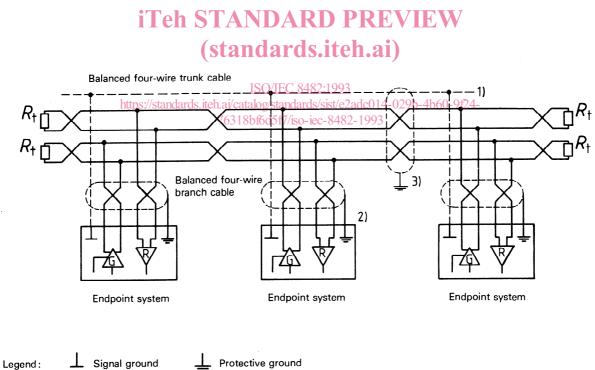


Figure 2 — Two-wire multipoint configuration



NOTES

- 1) Interconnection of the endpoint system signal ground is optional and depends on local regulations.
- 2) Branch cable shield is optional and, when provided, it connects to the endpoint system protective ground, which may be further connected to the signal ground.

3) Trunk cable shield is optional and, when provided, it connects to a protective ground at one place. Interconnection of shield to branch cable shields may be necessary.

Figure 3 — Four-wire multipoint configuration

6 Load on the multipoint medium

Each endpoint system represents a load to the multipoint medium. The load consists of a passive generator and/or a receiver with associated internal wiring and a balanced branch cable as shown in figures 2 and 3. In accordance with the multipoint half duplex data transmission principle, only one generator is in the active state at a given time.

Successful operation requires specification of the load in terms of d.c. loading and a.c. loading. For d.c. loading, the component specification in clauses 8 and 9 are selected such that an active generator can drive the interconnecting trunk cable, terminated at each end with not less than 120 Ω , and 32 so-called Unit Loads (ULs), representing the total load of all endpoint systems. The value of 1.0 UL is defined in 6.1.1.

6.1 Specification of d.c. loading

The d.c. loading specification limits the current of an active generator to a practical value. For this reason, a hypothetical Unit Load (UL) is defined for a current/voltage measurement. (standard

6.1.1 UL definition (see figure 4)

The value of 1,0 UL is defined by accurrent hanging g/standar The slopes of the currents should be positive to lower between - 0,8 mA and + 1,0 mA when varying the 6d5f7/isothe 84possibility of oscillations from negative voltage between - 7 V and + 12 V. The correspondent current/voltage diagram is shown in figure 4.

The voltage range takes into account the output and offset voltage of the generator, the common mode and internal voltage of the receiver and the power supply voltage.

UL determination of 6.1.2 the endpoint systems (see figures 5 and 6)

When measuring the current/voltage characteristics at the disconnected branch/trunk cable connector of one endpoint system, the measured generator shall be in the inactive state. The measurement configuration is shown in figure 5. The current/voltage measurement corresponds to that of the V.11 receiver input in ITU-T Recommendation V.11, i.e. with the voltage Via (or Vib) ranging between - 7 V and + 12 V, while V_{ib} (or V_{ia}) is held at zero volts, the resulting input current l_{ia} (or l_{ib}) should remain within the shaded range shown in figure 4. These measurements apply with the power supply of the generator and/or receiver in both the power-on and power-off conditions.

To determine UL from the measurements, the slope of the bounds of the current limit of one UL, see figure 4, shall be modified to the minimum slope required to fully contain the current/voltage characteristics, while the - 3 V and + 5 V intercept points are maintained. The actual value of UL is then equal to the larger of the two ratios of the actual current to the one UL current at the - 7 V and + 12 V points^C (see the two examples of UL value determinations in figure 6).

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resistance. When adding all measured UL values, the sum shall

6.2 a.c. loading

not exceed 32.0.

The a.c. loading on the multipoint medium affects the received signal quality. The determining factors, such as cable characteristics, type of encoding, etc., are

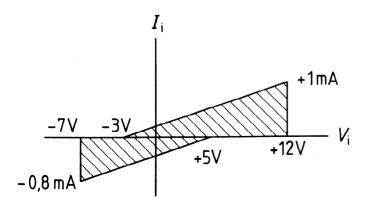


Figure 4 — Current limit of 1,0 UL

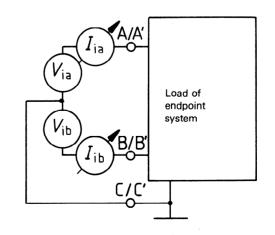


Figure 5 — Input current/voltage measurement

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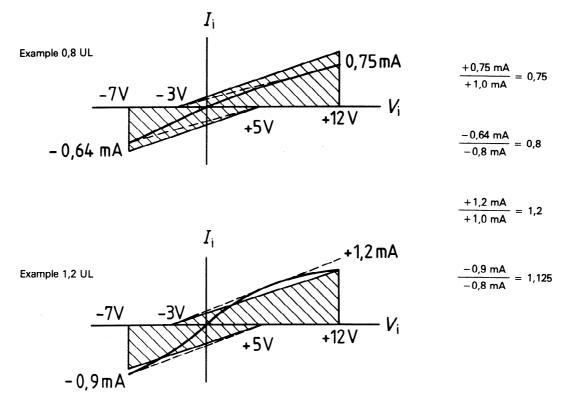


Figure 6 — UL value determination

application dependent and therefore beyond the RD The tests are made for either binary state, whereby scope of this International Standard. Some for the magnitude of the voltage specifications both guidance, however may be obtained form annex B. symbols |V| and $|\overline{V}|$ are used, respectively.

ISO/IEC 8482:198.1 Open circuit voltage, V

7 Polarities and significant levels atalog/standards/sist/e2adc014-029b-4b60-9f24-

The generator polarities and receiver significant levels have closer tolerances than those specified in ITU-T Recommendation V.11.

	$V_{\mathbf{A}'} - V_{\mathbf{B}'} \leq -0, 2V$	$V_{A'}$ - $V_{B'} \leq + 0, 2V$
Data circuits	MARK, 1	SPACE, 0
Control and timing circuits	OFF	ON

8 Generator characteristics

The generator component is measured in the active, low impedance state by the following tests using the measurement configurations shown in figures 7 to 10. The component may be operated from a singlerail positive power supply.

76318bf6d5f7/iso-iec-8The¹ voltage, when measured in accordance with significant figure 7, shall be, between the

- --- output terminals A, B: $1,5V \le |V_o|$ or $|\overline{V_o}| \le 6,0V$
- − terminals A, C and B, C: $|V_{oa}|$ or $|V_{ob}|$ or $|\overline{V}_{oa}|$ or $|\overline{V}_{ob}| \le 6,0 V$

8.2 Offset voltage, V_{os}

The voltage, when measured in accordance with figure 8, shall be, between the

- load centre and terminal C: $0V \le V_{os}$ or $\overline{V_{os}} \le 3,0V$ - binary states, the difference: $|V_{os} - \overline{V_{os}}| \le 0,2V$

8.3 Terminated output voltage, V,

The voltage, when measured in accordance with figure 9 by varying the testing voltage V in the range from - 7 V to + 12 V shall be, between the

— binary states, the difference: $|V_i| - |\overline{V_i}| \le 0.2V$

8.4 Rise time, t_r

When testing the mark/space reversals voltage V_{ss} in accordance with figure 10, the rise and fall time between 0,1 and 0,9 of V_{ss} on the output terminals A, B shall be

$$t_r \leq 0.3t_b$$

where

 $t_b = \text{time of UI (unit interval); and}$ $V_{ss} = |V_t - \overline{V_t}|$

- the resultant voltage due to imbalance between load centre and terminal C shall be

 $V_{e} \leq 0, 4V$ peak - to - peak.

9 Receiver characteristics

The receiver component is measured in accordance with the measurement configurations shown in DA figures 11 and 12.

A component meeting these requirements results in a different contention.)

differential receiver having a high input impedance, a

small input threshold transition region between SO/IEC 8481:1Environmental constraints

- 0,2 V and + 0,2 V differential, tand allowance tor an g/standards/sist/e2adc014-029b-4b60-9f24internal bias voltage not exceeding 5 V in magnifude: 16d5f7/iso-Incorder-1600 perate a balanced interchange circuit at

9.1 Input sensitivity (see figure 11)

The permitted range of input voltages $V_{A'}$ and $V_{B'}$ appearing at the receiver input terminals A' and B' measured with respect to receiver terminal C' shall be between - 7 V and + 12 V. For any combination of receiver input voltages within this permitted range, the receiver shall assume the intended binary state with an applied differential input voltage V_i of $\pm 0,2$ V or more.

9.2 Input balance (see figure 12)

The balance of the receiver input voltage/current characteristics and internal bias voltages shall be such that the receiver will remain in the intended binary state when a differential voltage V_{R3} of \pm 0,4 V is applied through matched resistors equal to 1 500 Ω to each input terminal, as shown in figure 12, with the input voltages V_{R1} and V_{R2} ranging between -7 V and + 12 V. When the polarity of V_{R3} reverses, the opposite binary state shall be maintained under the same conditions.

10 Fault condition tests

In order to ensure no damage occurs due to a single fault condition the components shall be tested in accordance with the measurement configurations shown in figures 13 to 14.

10.1 Generator short circuit (see figure 13)

A generator shall not sustain any damage as a result of short-circuiting its output terminals A and B to each other.

10.2 Generator current limitation (see figure 14)

The peak current in any lead to the generator shall not exceed 250 mA when testing in accordance with figure 14 by varying the testing voltage V in the range from - 7 V to + 12 V.

This criterion should not be interpreted as a requirement that a generator be capable of sourcing 250 mA. The sinking generator shall not permit a composite current in excess of 250 mA, if multiple (sourcing) generators are providing that current. (See annex A clause A.4 for additional information on generator contention.)

Hnorder-to operate a balanced interchange circuit at data signalling rates up to 12,5 Mbit/s, the following conditions apply:

The total common-mode voltage at any point of the interchange circuit shall be within - 7 V to + 12 V.

The common mode voltage at the receiver is the worst case combination of

a) generator-receiver ground potential difference ($V_{e'}$, see figure 1);

b) longitudinally induced random noise voltage measured between the receiver terminals A' or B' and C' with the generator ends of the cable A, B, and C joined together;

c) generator offset voltage $V_{as'}$.

12 Component compatibility

Generators and receivers meeting the requirements of this International Standard will meet the requirements of ITU-T Recommendation V.11.

Characteristics	ISO/IEC 8482	ITU-T Recommendation V.11	
Generator and receiver			
Power supply Common mode	positive - 7V to + 12 V	positive and/or negative - 7 V to + 7 V	
Generator			
Generator			
Open circuit	≤ 6,0 V	≤ 6,0 V	
Output terminated	1,5 V to 5,0 V/54 Ω	2,0 V to 6,0 V/100 Ω	
Offset	≤ 3,0 V	≤ 3,0 V	
Mark/Space difference	≤ 0,2 V	≤ 0,4 V	
Rise/Fall time	≤ 0,3 UI	≤ 0,1 UI	
Imbalance	not specified	≤ 0,4 V p/p	
Short circuit	not specified	≤ 150 mA	
Current limitation	≤ 250 mA	not specified	
Receiver			
Sensitivity min. iTeh S		± 300 mV	
Sensitivity range	- 7 V to + 12 V	- 10 V to + 10 V	
Imbalance (§	##00mards.it	e±720 mV	
Internal bias	≤ 5,0 V	≤ 3,0 V	
Failure detection	not specified 8482:199	3 ³ types	
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76318bf6d5f7/iso-iec-8482-1993			
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	0		

Table 2 - Compatibility with ITU-T Recommendation V.11



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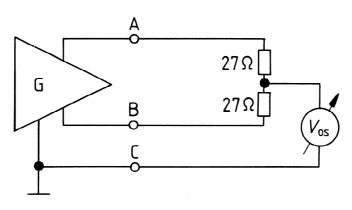


Figure 8 — Offset voltage measurement