

Edition 2.0 2016-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices – W Part 6-13: Design guideline of open-top-type sockets for Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA)

Normalisation mécanique des dispositifs à semiconducteurs – Partie 6-13: Guide de conception pour les supports sans couvercle pour les boîtiers matriciels à billes et à pas fins (FBGA) et les boîtiers matriciels à zone de contact plate et à pas fins (FLGA)





THIS PUBLICATION IS COPYRIGHT PROTECTED Copyright © 2016 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

Droits de reproduction réservés. Sauf indication contraire, aucune partie de cette publication ne peut être reproduite ni utilisée sous quelque forme que ce soit et par aucun procédé, électronique ou mécanique, y compris la photocopie et les microfilms, sans l'accord écrit de l'IEC ou du Comité national de l'IEC du pays du demandeur. Si vous avez des questions sur le copyright de l'IEC ou si vous désirez obtenir des droits supplémentaires sur cette publication, utilisez les coordonnées ci-après ou contactez le Comité national de l'IEC de votre pays de résidence.

IEC Central Office	Tel.: +41 22 919 02 11
3, rue de Varembé	Fax: +41 22 919 03 00
CH-1211 Geneva 20	info@iec.ch
Switzerland	www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

IEC Catalogue - webstore.iec.ch/catalogue

The stand-alone application for consulting the entire bibliographical information on IEC International Standards, Technical Specifications, Technical Reports and other documents. Available for PC, Mac OS, Android Tablets and iPad.

IEC publications search - www.iec.ch/searchpub

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and also once a month by email.

Electropedia - www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing 20/000 terms and definitions in English and French, with equivalent terms in 15 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary

653000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

IEC Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.

A propos de l'IEC

La Commission Electrotechnique Internationale (IEC) est la première organisation mondiale qui élabore et publie des Normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications IEC

Le contenu technique des publications IEC est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

Catalogue IEC - webstore.iec.ch/catalogue

Application autonome pour consulter tous les renseignements bibliographiques sur les Normes internationales, Spécifications techniques, Rapports techniques et autres documents de l'IEC. Disponible pour PC, Mac OS, tablettes Android et iPad.

Recherche de publications IEC - www.iec.ch/searchpub

La recherche avancée permet de trouver des publications IEC en utilisant différents critères (numéro de référence, texte, comité d'études,...). Elle donne aussi des informations sur les projets et les publications remplacées ou retirées.

IEC Just Published - webstore.iec.ch/justpublished

Restez informé sur les nouvelles publications IEC. Just Published détaille les nouvelles publications parues. Disponible en ligne et aussi une fois par mois par email.

Electropedia - www.electropedia.org

Le premier dictionnaire en ligne de termes électroniques et électriques. Il contient 20 000 termes et définitions en anglais et en français, ainsi que les termes équivalents dans 15 langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International (IEV) en ligne.

Glossaire IEC - std.iec.ch/glossary

65 000 entrées terminologiques électrotechniques, en anglais et en français, extraites des articles Termes et Définitions des publications IEC parues depuis 2002. Plus certaines entrées antérieures extraites des publications des CE 37, 77, 86 et CISPR de l'IEC.

Service Clients - webstore.iec.ch/csc

Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions contactez-nous: csc@iec.ch.



Edition 2.0 2016-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices - W Part 6-13: Design guideline of open-top-type sockets for Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA)

IEC 60191-6-13:2016

Normalisation mécanique des dispositifs à semiconducteurs -Partie 6-13: Guide de conception pour les supports sans couvercle pour les boîtiers matriciels à billes et à pas fins (FBGA) et les boîtiers matriciels à zone de contact plate et à pas fins (FLGA)

INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

ICS 31.080.01

ISBN 978-2-8322-3662-8

Warning! Make sure that you obtained this publication from an authorized distributor. Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

 Registered trademark of the International Electrotechnical Commission Marque déposée de la Commission Electrotechnique Internationale

CONTENTS

F	OREWC	RD	3		
IN	ITRODU	ICTION	5		
1	Scop	e	6		
2	2 Normative references				
3	Term	s and definitions	6		
4	Sock	et code	6		
	4.1	Construction of socket code	6		
	4.2	Symbols	7		
	4.2.1	Semiconductor sockets symbol	7		
	4.2.2		7		
	4.2.3	,			
	4.2.4	5			
	4.2.5				
5		inal number			
6		et nominal dimension			
7		et length and width			
8	Refe	rence symbols and schematics DARD PREVIEW	8		
	8.1	Outline drawings Reference symbols and schematics of recommended socket mounting	8		
	8.2	Reference symbols and schematics of recommended socket mounting	11		
	8.3	pattern on printed circuit board Overall dimensions <u>IFC.60191-6-13:2016</u>			
	8.4	Recommended dimensions of socket mounting pattern on printed circuit	12		
	0.4	board	17		
9	Indiv	idual outline drawing standard registration	18		
Fi	gure 1 -	- Outline drawings of the socket	9		
Figure 2 – Outline drawings for the definition of terminal diameter					
	-	- Applicable package outline			
	Figure 4 – Socket mounting pattern				
• •	9				
Та	able 1 –	Overview for the different socket groups	8		
Та	able 2 –	Overall dimensions (1 of 2)	12		
		Socket dimensions for Group 1, 2 and 3 (square socket) (1 of 2)			
		Socket dimension for Group 4 (square or rectangular socket)			
		Socket mounting dimensions			
		Registration table			

INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-13: Design guideline of open-top-type sockets for Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA)

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user. (Standards.iten.al)
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter. https://standards.iteh.ai/catalog/standards/sist/a821323d-c750-4cdc-84a3-
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-13 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2007. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) BGA package nominal length and width have been newly expanded to 43 mm and 43 mm, respectively. Accordingly, six socket sizes have been added to the socket group numbers 1, 2 and 3, and twenty-two socket sizes have been added to the socket group number 4.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/878/FDIS	47D/885/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical* standardization of semiconductor devices, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>IEC 60191-6-13:2016</u> https://standards.iteh.ai/catalog/standards/sist/a821323d-c750-4cdc-84a3d4966cfdda69/iec-60191-6-13-2016

INTRODUCTION

This part of IEC 60191 aims to standardize the outer dimensions of the sockets for FBGA and FLGA, where leading-edge developments are aggressively innovated, to establish their compatibility with the needs of the surface-mount industry that is globally expanding due to enhanced functions and performances of electrical devices.

For defining each dimension, the target was to indicate the standard design value which has the concept of the design centre as much as possible, aiming to enhance the function as a standardization index.

iTeh STANDARD PREVIEW (standards.iteh.ai)

<u>IEC 60191-6-13:2016</u> https://standards.iteh.ai/catalog/standards/sist/a821323d-c750-4cdc-84a3d4966cfdda69/iec-60191-6-13-2016

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-13: Design guideline of open-top-type sockets for Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA)

1 Scope

This part of IEC 60191 specifies a design guideline of open-top-type semiconductor sockets for Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA). In particular, this part of IEC 60191 establishes the outline drawings and dimensions of the open-top-type test and burn-in sockets applied to FBGA and FLGA.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-2, Mechanical standardization of semiconductor devices – Part 2: Dimensions

IEC 60191-6, Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

<u>IEC 60191-6-13:2016</u>
 Terms and definitions <u>4966cfdda69/iec-60191-6-13-2016</u>

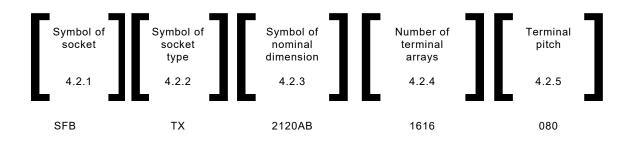
For the purposes of this document, the terms and definitions given in IEC 60191-6 apply.

4 Socket code

4.1 Construction of socket code

A socket code is constructed as follows.

EXAMPLE



4.2 Symbols

4.2.1 Semiconductor sockets symbol

The symbol for socket shall be expressed in three characters. The first character, "S", refers to socket and the rest to the package code. FBGA shall be expressed as "FB", FLGA shall be expressed as "FL".

4.2.2 Socket type symbol

The symbol for socket type shall be expressed in two characters. The first character "T" refers to open-top type and the rest remains option "X". Clamshell type socket is referred to as "C".

4.2.3 Socket nominal dimension symbol

The symbol for nominal dimension shall be expressed in six characters, which consist of four numeric characters and two alphabetical characters. The first four numeric characters comply with nominal dimension $E \times D$, which refers to the applicable maximum width and length of FBGA/FLGA package.

The last two alphabetical characters refer to socket base matrix size either an even or an odd.

It refers to an odd contact row by "A" and an even contact row by "B" in the following order: socket width direction and then socket length direction.

Namely, it refers to "AA" in case row number is an odd number both for width and length direction, "BB" in case row number is an even number both for width and length direction, "AB" in case row number is an odd number for width direction and an even number for length direction, and "BA" in case row number is an even number for width direction and an odd

number for length direction. <u>IEC 00191-0-132010</u> https://standards.iteh.ai/catalog/standards/sist/a821323d-c750-4cdc-84a3-

d4966cfdda69/iec-60191-6-13-2016

4.2.4 Number of terminal arrays

The symbol for the number of terminal arrays shall be expressed by four numeric characters applying applicable package matrix size in the E direction and the D direction.

4.2.5 Terminal pitch

The symbol for terminal pitch of applicable package shall be expressed in three numeric characters. The decimal sign is omitted.

5 Terminal number

The terminal number is provided in the following manner when the socket is viewed with the angle from topside. The horizontal row nearest to the index corner when the index is placed on the left topside is referred to as A.

As the row moves down, the number changes in the order of B, C, AA, AB.

The terminal number one (1) is defined for the vertical row nearest to the index corner. As the row moves rightward, the number is increased to two (2), three (3), etc. The terminal number is combined with these letters and numbers and expressed as A1 or B1. Six (6) alphabetical letters, "I", "O", "Q", "S", "X" and "Z", shall not be used as symbols for a horizontal row.

6 Socket nominal dimension

The applicable package length and width which extend from 1,50 mm to 43,0 mm by 0,50 mm increments are divided into ten package groups. The socket nominal dimension is defined by the largest value of the package length or width in each socket group.

In consideration of a specific need for minimum socket outline size, the socket nominal dimension with 1,0 mm increments can be specified as an exception. The package length and width of 5,00 mm or less are unified in one socket nominal dimension.

7 Socket length and width

Socket length and width are categorized into four groups, from group one (1) to group four (4), to cover the difference of its terminal counts and mechanism (see Table 1).

In socket group one (1), two (2) and three (3), only the square socket outline is allowed. Socket length and width are determined by the nominal dimension value plus 36,0 mm, 24,0 mm and 12,0 mm, respectively.

In socket group four (4), square and rectangular socket outlines are allowed. Socket length and width are determined by the nominal dimension value plus 8,0 mm independently in each side.

Socket group one (1) is intended for a high terminal counts package or a FLGA socket which is composed of a complicated socket structure. Socket groups two (2) and three (3) are for the socket currently available. Socket group four (4) is for the socket which is required to have the smallest possible outline, such as for Memory IC.

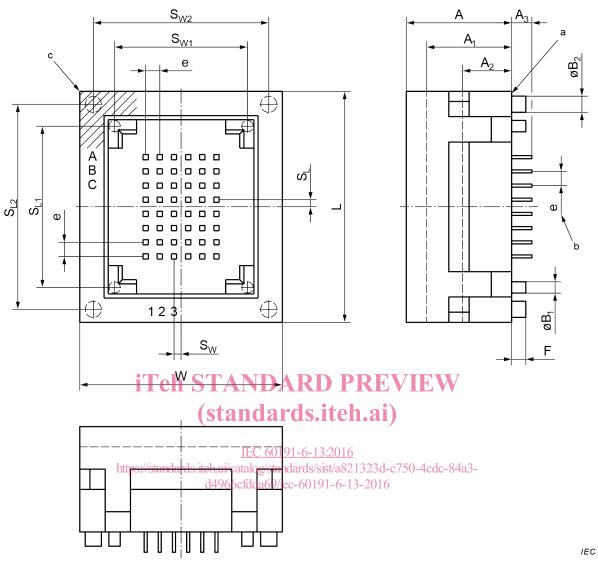
http://standards.ic.h.ai/catalog/standards/ist/a821323d-c750-4cdc.84a3d4966ctdda69/iec-60191-6-13-2016

Socket group number	Allowed socket outline	Value added to the socket nominal dimension to determine the socket length and width
Group 1	Square	36,0 mm
Group 2	Square	24,0 mm
Group 3	Square	12,0 mm
Group 4	Square or rectangular	8,0 mm

8 Reference symbols and schematics

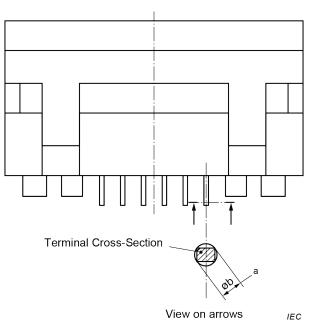
8.1 Outline drawings

Outline drawings of the socket and the terminal diameter are shown in Figure 1 and Figure 2, respectively. The applicable package outline is presented in Figure 3. The overall dimensions are given in Table 2 and socket dimensions in Table 3 and Table 4.



- ^a Indicates the mounting plane. The mounting plane is defined by the plane where the socket contacts its mounting surface.
- ^b Stipulates the true geometric position of the terminals.
- ^c Indicates positional tolerance of the index mark. Index mark should be completely within the shaded area.

Figure 1 – Outline drawings of the socket



^a Terminal diameter is defined as the maximum diameter of a circle circumscribed about a horizontal cross-section of the terminal from the mounting plane.

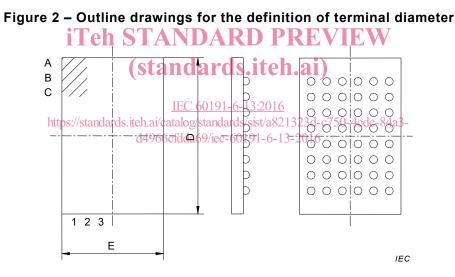
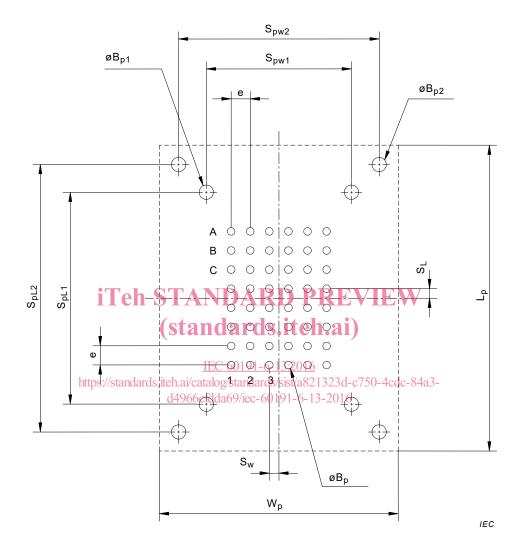


Figure 3 – Applicable package outline

8.2 Reference symbols and schematics of recommended socket mounting pattern on printed circuit board

The drawing of the recommended socket mounting pattern on a printed circuit board is shown in Figure 4 for reference in designing printed circuit board. See Table 5 for recommended dimensions.



NOTE The subscript "p" indicates projected dimension. For example, L_p is recognized automatically as the projected dimension "L" to the base plane.

Figure 4 – Socket mounting pattern