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Edition 1.0 2016-03

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Dynamic modules –
Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

Modules dynamiques –
Partie 4-1: Interface logicielle et matérielle – Commutateur sélectif en longueur d'onde 1 x 9

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DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

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The text of this standard is based on the following documents:

CDV	Report on voting
86C/1304/CDV	86C/1346/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62343 series, published under the general title *Dynamic modules*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

A wavelength selective switch (WSS) is a dynamic module, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch all wavelength signals to their respective required output port in dense wavelength division multiplexing (DWDM) networks. The WSS module has one input port and a plurality of output ports (i.e. 1 x N WSS) and can be used reversely, such as N input ports and one output port, depending on its application. It is electrically controlled with software, which directs each wavelength signal among an input DWDM signal from one input port to the required output port for each wavelength signal.

DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

1 Scope

This part of IEC 62343 describes and provides specifications for a software and hardware interface for the 1 x 9 wavelength selective switch.

These switches can be controlled by resident firmware with this interface. This standard addresses the configuration and function to control a WSS. This interface is intended to enable a user or host to retrieve the switch status and/or adjust relevant switch and attenuation settings.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication* (available at http://www.electropedia.org)

IEC 62343, *Dynamic modules - General and guidance*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731 and IEC 62343, as well as the following apply.

3.1.1
wavelength selective switch
WSS
dynamic module with one or more input ports and one or more output ports, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch each wavelength signal on each input port independently to its required output port in DWDM networks

Note 1 to entry: It is electrically controlled with software.

Note 2 to entry: It can be used inverted, exchanging input and output ports.

Note 3 to entry: Each wavelength signal can be independently attenuated.

3.2 Abbreviations

For the purposes of this document, the following abbreviations apply.

DWDM dense wavelength division multiplexing

WSS wavelength selective switch

ROADM	reconfigurable optical add drop multiplexer
HC	host controller
DPRAM	dual-port RAM
FPGA	field programmable gate array
DSP	digital signal processor
R/W	read or write
RW	read and write
RO	read only
CE	chip enable
OE	output enable
TxD	transmitted data
RxD	received data

4 Basic configuration of WSS interface

The software interface is intended to provide an access to the functions of the WSS module and be the primary interface to command the unit. The HC controls the WSS module by sending control signal, as well as command data, to the WSS module via a 12-bit address bus, a 16-bit data bus, and DPRAM related signal lines such as Read/Write, Chip Enable, and Output Enable. The HC also receives from the WSS module response signals and status data.

Any address within the DPRAM can be written to via the HC, however many of these values will be overwritten upon the application of a command to the WSS module. The addresses, which are identified as inputs, can be found further along in this document. In addition to the DPRAM interface, RS232 serial communication is also supported by the WSS module.

The WSS module has a non-volatile memory to store the latest setting when requested. A functional diagram of the WSS module controls is illustrated in Figure 1 below.

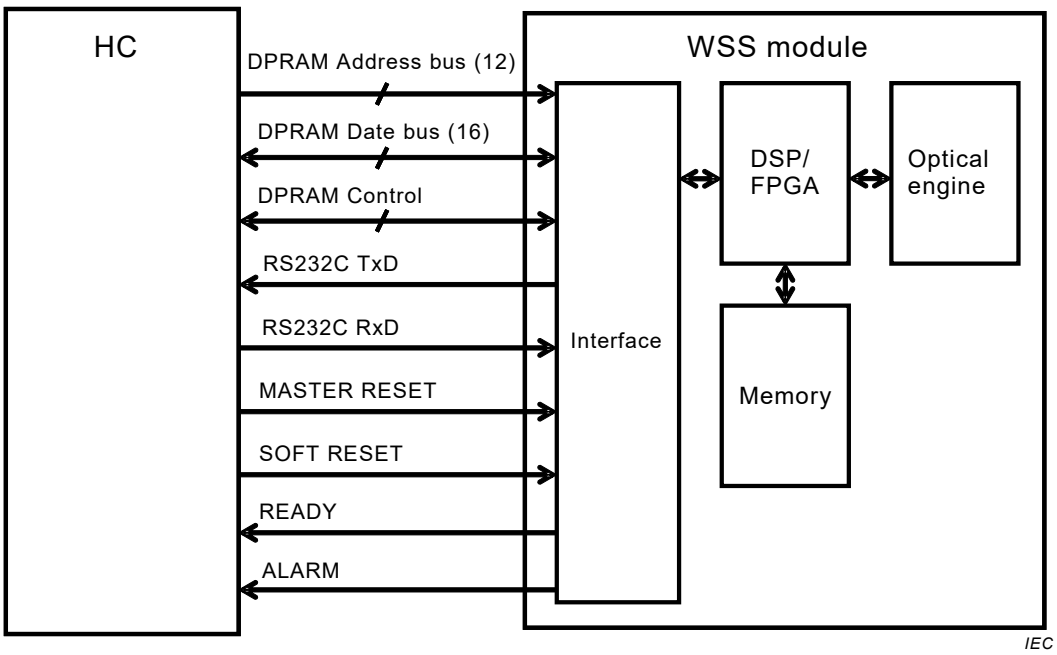

Figure 1 – Basic configuration of WSS interface

5 Software interface

The signals between the HC and the WSS module are low voltage +3,3 V logic levels. The definitions of the signals and memory map are described in Table 1 and Table 2. Annex A provides additional information on pin assignment. Annex B provides additional information DPRAM memory map and timing charts.

Table 1 – Software interface

No	Functional block	Name	Input/output	Definitions
1	DPRAM	Address (12-bit wide)	Input	12-bit address bus of DPRAM.
		Data (16-bit wide)	Input/output	16-bit wide data bus of DPRAM.
		START	Input	WSS module start input signal. This strobe is generated by the HC to command the WSS module to perform a specified task defined in command word 2. This signal is an active low input signal.
		DONE	Output	Done output signal. A level high is generated by the WSS module when a specified task is completed.
		ERROR	Output	Error output signal. A level high is generated by the WSS module when it detects an error condition.
		BUSY	Output	Busy output signal. This signal indicates that both the WSS module and HC are trying to access the same dual port RAM address at the same time. This signal is an active low signal.
				Read/write enable (R/W) input signal. This signal is generated by the HC to enable reading of data from dual port RAM, or writing of data to dual port RAM.
				Chip enable (CE) input signal. This signal is generated by the HC to select the dual port RAM devices. This signal is an active low signal.

No	Functional block	Name	Input/output	Definitions
				Chip output enable (OE) input signal. This signal is generated by the HC to enable the dual port RAM to send out data on the data bus. This signal is an active low signal.
2	RS232C	TxD	Output	Transmitted data (TxD): This signal is active when data is transmitted from the WSS module to the HC. When no data is transmitted, the signal is held in the mark condition.
		RxD	Input	Received data (RxD): This signal is active when the WSS module receives data from the HC. When no data is transmitted, the signal is held in the mark condition.
3	Module control	MASTER RESET	Input	Input signal. This strobe is generated by the HC to command the WSS module to perform Master reset which affects optical configurations of the module. This signal is an active low input signal.
		SOFT RESET	Input	Input signal. This resets the WSS module DSP without affecting optical state of the WSS module. This signal is an active low input signal.
		READY	Output	This signal is asserted (logic '0') by the WSS module to inform the HC that transmission may begin.
		ALARM	Output	This signal is generated by the WSS module when a hardware alarm or a software alarm is generated.

Table 2 – DPRAM memory map

No.	Address	Content	R/W	Notes
1	0x0001	Hardware and software version	RO	The hardware and software versions are embedded.
2	0x0020	Command register	RW	
3	0x0021	Command code register	RW	
4	0x0022	Command data 1 register	RW	
5	0x0023	Status register	RW	
6	0x0025	Error code register	RW	
7	0x0028	WSS case temperature	RO	
8	0x0029	Hardware error register	RO	
9	0x0034	Command data 2 register	RW	
10	0x0035	Command data 3 register	RW	

6 Hardware interface – Electrical connector

The electrical connector on the WSS module is an 80-contact receptacle. Annex A provides additional information on connector form.

Annex A
(informative)

Hardware interface details

Annex A describes two kinds of interfaces. All specifications in Annex A are informative. It is recommended that the user chooses either connector form A or B. Table A.1 gives details on connector form, Table A.2 on pin assignment, Table A.3 on the supply voltages and currents for WSS module, Table A.4 on low voltage TTL thresholds and Table A.5 on power consumption.

Table A.1 – Connector form

No	Parameter	Connector form A	Connector form B
1	Connector form	Samtec CLT-140-02-G-D-BE-A	Samtec CLP-140-02-S-D

Table A.2 – Pin assignment

No	Functional block	Name	Pin assignment A	Pin assignment B
1	Dual port RAM	Address (12-bit wide)	Address bit 0 to 11, pin 51 to 62	DPRA 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 Pin 70, 68, 66, 64, 62, 60, 58, 56, 54, 52, 48
		Data (16-bit wide)	Data bit 0 to 15, pin 1 to 16	DPRD 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15 Pin 44, 42, 40, 38, 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16, 14
		START	START, pin 21	nSTART, pin 27
		DONE	DONE, pin 23	DONE, pin 25
		ERROR	ERROR, pin 25	ERROR, pin 23
		BUSY	BUSY, pin 26, low	nBUSY, pin 29
		Read Write from RAM	Read Write from RAM, pin 45	R/nW, pin 15
		RAM Chip Enable	RAM Chip Enable, pin 47	nCE, pin 13
		RAM Chip Output Enable	RAM Chip Output Enable, pin 48	nOE, pin 17
2	RS232C	TxD	TxD, pin 65	TxD, pin 51
		RxD	RxD, pin 66	RxD, pin 53
3	Module control	MASTER RESET	MASTER RESET, pin 19	nRST, pin 74
		SOFT RESET	HARD RESET, pin 46	nSWRST, pin 67
		READY	CTS, pin 20	nREADY, pin 61
		ALARM	WDERR, pin 24	ALARM, pin 31 or nFAULT, pin 33

Table A.3 – Supply voltages and currents

No	Parameter	Supply voltage and current A			Supply voltage and current B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
1	Supply voltage +3,3 V	+3,14	+3,3	+3,5	NA	NA	NA	V
2	Supply voltage +5,0 V	+4,75	+5,0	+5,25	+4,75	+5,0	+5,6	V
3	Supply voltage +5,0 V-Analog	+4,75	+5,0	+5,25	+4,75	+5,0	+5,6	V
4	Supply voltage +15,0 V-Analog	+14,25	+15,0	+15,75	NA	NA	NA	V
5	Supply voltage -15,0 V-Analog	-15,75	-15,0	-14,25	NA	NA	NA	V
6	Supply current +3,3 V	NA	NA	+3,0	NA	NA	NA	A
7	Supply current +5,0 V	NA	NA	+2,0	NA	NA	+7,0	A
8	Supply current +5,0 V-Analog	NA	NA	+2,0	NA	NA	NA	A
9	Supply current +15,0 V-Analog	NA	NA	+1,0	NA	NA	NA	A
10	Supply current -15,0 V-Analog	NA	NA	1,0	NA	NA	NA	A

All the WSS control signals are LVTTL CMOS (3,3 V). The voltage level thresholds are as specified in Table A.4 below.

Table A.4 – Low voltage TTL thresholds

No	Parameter	Low voltage TTL thresholds A		Low voltage TTL thresholds B		Unit
		Min.	Max.	Min.	Max.	
1	Logic low input level	NA	+0,8	-0,2	+0,8	V
2	Logic high input level	+2,0	+5,5	+2,0	+3,45	V
3	Logic low output level	NA	+0,4	NA	+0,4	V
4	Logic high output level	+2,4	+3,3	+2,8	NA	V

Table A.5 – Power consumption

No	Parameter	Power consumption A	Power consumption B	Unit
		Max.	Max.	
1	Power consumption	10	33[a]	W

[a] Including warm-up.