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INTERNATIONAL STANDARD

Dynamic modules –
Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

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DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

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International Standard IEC 62343-4-1 has been prepared by subcommittee SC86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics.

The text of this standard is based on the following documents:

CDV	Report on voting
86C/1304/CDV	86C/1346/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62343 series, published under the general title *Dynamic modules*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

A wavelength selective switch (WSS) is a dynamic module, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch all wavelength signals to their respective required output port in dense wavelength division multiplexing (DWDM) networks. The WSS module has one input port and a plurality of output ports (i.e. 1 x N WSS) and can be used reversely, such as N input ports and one output port, depending on its application. It is electrically controlled with software, which directs each wavelength signal among an input DWDM signal from one input port to the required output port for each wavelength signal.

DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

1 Scope

This part of IEC 62343 describes and provides specifications for a software and hardware interface for the 1 x 9 wavelength selective switch.

These switches can be controlled by resident firmware with this interface. This standard addresses the configuration and function to control a WSS. This interface is intended to enable a user or host to retrieve the switch status and/or adjust relevant switch and attenuation settings.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication* (available at http://www.electropedia.org)

IEC 62343, *Dynamic modules - General and guidance*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731 and IEC 62343, as well as the following apply.

3.1.1
wavelength selective switch
WSS
dynamic module with one or more input ports and one or more output ports, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch each wavelength signal on each input port independently to its required output port in DWDM networks

Note 1 to entry: It is electrically controlled with software.

Note 2 to entry: It can be used inverted, exchanging input and output ports.

Note 3 to entry: Each wavelength signal can be independently attenuated.

3.2 Abbreviations

For the purposes of this document, the following abbreviations apply.

DWDM dense wavelength division multiplexing
WSS wavelength selective switch

ROADM	reconfigurable optical add drop multiplexer
HC	host controller
DPRAM	dual-port RAM
FPGA	field programmable gate array
DSP	digital signal processor
R/W	read or write
RW	read and write
RO	read only
CE	chip enable
OE	output enable
TxD	transmitted data
RxD	received data

4 Basic configuration of WSS interface

The software interface is intended to provide an access to the functions of the WSS module and be the primary interface to command the unit. The HC controls the WSS module by sending control signal, as well as command data, to the WSS module via a 12-bit address bus, a 16-bit data bus, and DPRAM related signal lines such as Read/Write, Chip Enable, and Output Enable. The HC also receives from the WSS module response signals and status data.

Any address within the DPRAM can be written to via the HC, however many of these values will be overwritten upon the application of a command to the WSS module. The addresses, which are identified as inputs, can be found further along in this document. In addition to the DPRAM interface, RS232 serial communication is also supported by the WSS module.

The WSS module has a non-volatile memory to store the latest setting when requested. A functional diagram of the WSS module controls is illustrated in Figure 1 below.

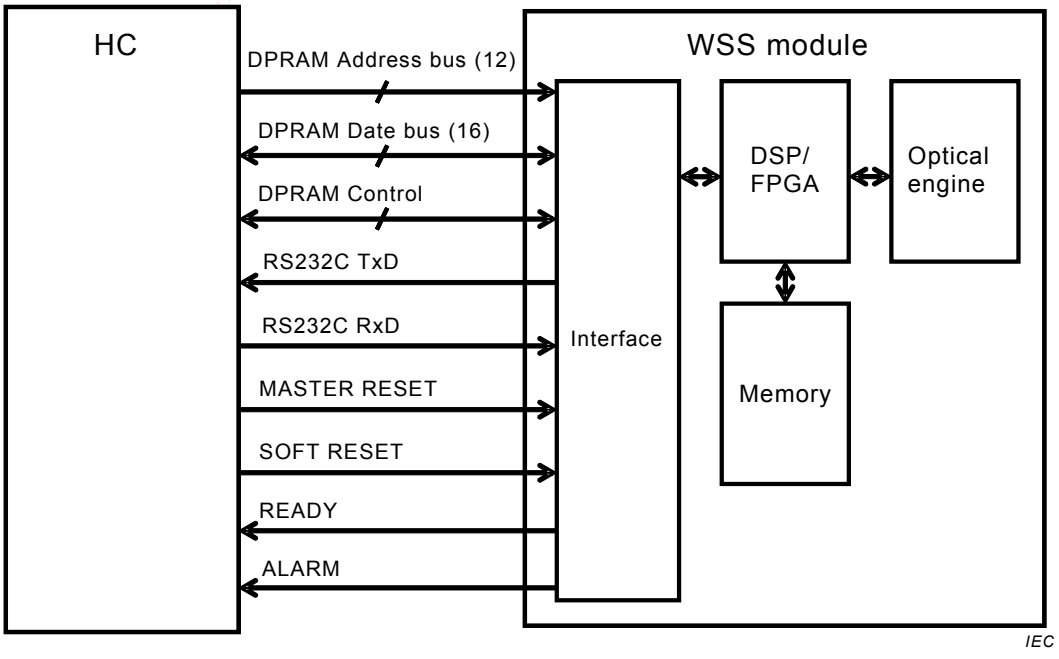

Figure 1 – Basic configuration of WSS interface

5 Software interface

The signals between the HC and the WSS module are low voltage +3,3 V logic levels. The definitions of the signals and memory map are described in Table 1 and Table 2. Annex A provides additional information on pin assignment. Annex B provides additional information DPRAM memory map and timing charts.

Table 1 – Software interface

No	Functional block	Name	Input/output	Definitions
1	DPRAM	Address (12-bit wide)	Input	12-bit address bus of DPRAM.
		Data (16-bit wide)	Input/output	16-bit wide data bus of DPRAM.
		START	Input	WSS module start input signal. This strobe is generated by the HC to command the WSS module to perform a specified task defined in command word 2. This signal is an active low input signal.
		DONE	Output	Done output signal. A level high is generated by the WSS module when a specified task is completed.
		ERROR	Output	Error output signal. A level high is generated by the WSS module when it detects an error condition.
		BUSY	Output	Busy output signal. This signal indicates that both the WSS module and HC are trying to access the same dual port RAM address at the same time. This signal is an active low signal.
				Read/write enable (R/W) input signal. This signal is generated by the HC to enable reading of data from dual port RAM, or writing of data to dual port RAM.
				Chip enable (CE) input signal. This signal is generated by the HC to select the dual port RAM devices. This signal is an active low signal.