IEC 62889

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INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Digital video interface – Gigabit video interface for multimedia systems

Interface vidéo numérique – Interface vidéo gigabit pour les systèmes multimédias

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CONTENTS

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DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

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The text of this standard is based on the following documents:

CDV	Report on voting
100/2193/CDV	100/2298/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

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- amended.

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INTRODUCTION

This International Standard is based on a standard JEITA CP-6101: Digital monitor interface GVIF that was originally specified by the Japan Electronics and Information Technology Industries Association (JEITA).

The gigabit video interface (GVIF) is a serial point to point interface supporting uncompressed digital video links that was designed to address the needs of automotive navigation and entertainment systems, etc., to transport base band digital video information. The GVIF applies low voltage differential signaling (LVDS) technology and makes use of a thin cable consisting of a single shielded twisted pair of conductors that exhibits high noise immunity and low EMI, and is optimized for small size and low weight. The GVIF supports display resolutions ranging from WQVGA through WUXGA with maximum 24 bit per pixel colour video data, and can transmit base band video signal over cable lengths over 10 m. When paired with high bandwidth data content protection (HDCP), the GVIF's standard functions and features address all of the requirements for delivering content protected video from a source to a video display monitor. Optionally, the GVIF supports audio data transmission and user data transmission.

The Association of Radio Industry Business (ARIB) refers the GVIF in its standard ARIB STD-B21 as one of authorized digital video output interfaces.

DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

1 Scope

This International Standard describes a serial digital interface, gigabit video interface (GVIF) for the interconnection of digital video equipment. The GVIF is primarily intended to carry high-speed digital video data for general usage and is well suited for multimedia entertainment systems in a vehicle.

This International Standard specifies the physical layer of the interface including transmission line characteristics and electrical characteristics of transmitter and receiver. Mechanical and physical specifications of connectors are not included.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62315-1:2003, *DTV profiles for uncompressed digital video interfaces – Part 1: General*

ITU-R BT.601-5, *Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios*

ITU-R BT.656-5, *Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1.1
DE
display enable signal given in IEC 62315-1

3.1.2
HSYNC
display horizontal synchronous signal given in IEC 62315-1

3.1.3
VSYNC
display vertical synchronous signal given in IEC 62315-1

3.1.4
RGB
display red, green, blue colour data input (TX) or output (RX) given in ITU-R BT.601-5 and ITU-R BT.656-5

3.1.5
YU(Cb)V(Cr)
display Y, U (Cb), V (Cr) pixel data input (TX) or output (RX) given in ITU-R BT.601-5 and ITU-R BT.656-5

3.1.6
CNTL/AUX
down-stream user defined signal or audio enable signal

3.1.7
P[23:0]
digital signal data like a 24 bit colour video data such as RGB or YU (Cb) V (Cr) data input (TX) or output (RX)

3.1.8
GVIF RX
circuit that receives the serial signal from a shielded-pair transmission line, decodes them and outputs to convert into the parallel video signal

3.1.9
GVIF TX
circuit that receives the parallel video signal, the control signals, and encodes them into serial data to send a signal by driving a shielded-pair transmission line

3.1.10
LOS
loss of signal
detection signal, asserted when the differential input signal at the receiver cannot receive

3.1.11
RX front-end
front-end block of receiver side

3.1.12
SDA
serial data
down-stream signal

3.1.13
SDATAP
down-stream positive-phase side signal of the differential serial data

3.1.14
SDATAN
down-stream negative-phase side signal of the differential serial data

3.1.15
REFRQP
current source signal for reference clock request from Rx side

3.1.16
REFRQN
current source signal for reference clock request from Rx side as well as REFRQP

3.1.17
SFTCLK
pixel clock
clock for capture of the parallel video data per pixel

3.1.18
TDA
transmit data
down-stream user defined signal

3.1.19
TX front-end
front-end block of transmitter side

3.1.20
UDA
user data
up-stream user defined signal

3.1.21
IRQ
up-stream common-mode reference request current for REFRQP/N

3.1.22
VOS
common-mode voltage amplitude of reference request

3.1.23
VOD
differential voltage amplitude for SDATAP/N

3.1.24
VDD
power supply on the transmitter side

3.1.25
V_SDATAP
single-ended voltage of SDATAP

3.1.26
V_SDATAN
single-ended voltage of SDATAN

3.1.27
TP1
transmitter end point for eye mask specification

3.1.28
normalized differential voltage
voltage of transmitter output point

3.1.29
UI
normalized time unit interval of transmitter output point

3.2 Abbreviations

AC	Alternating Current
DC	Direct Current
EMI	Electro-Magnetic Interference
GVIF	Gigabit Video InterFace
LSB	Least Significant Bit

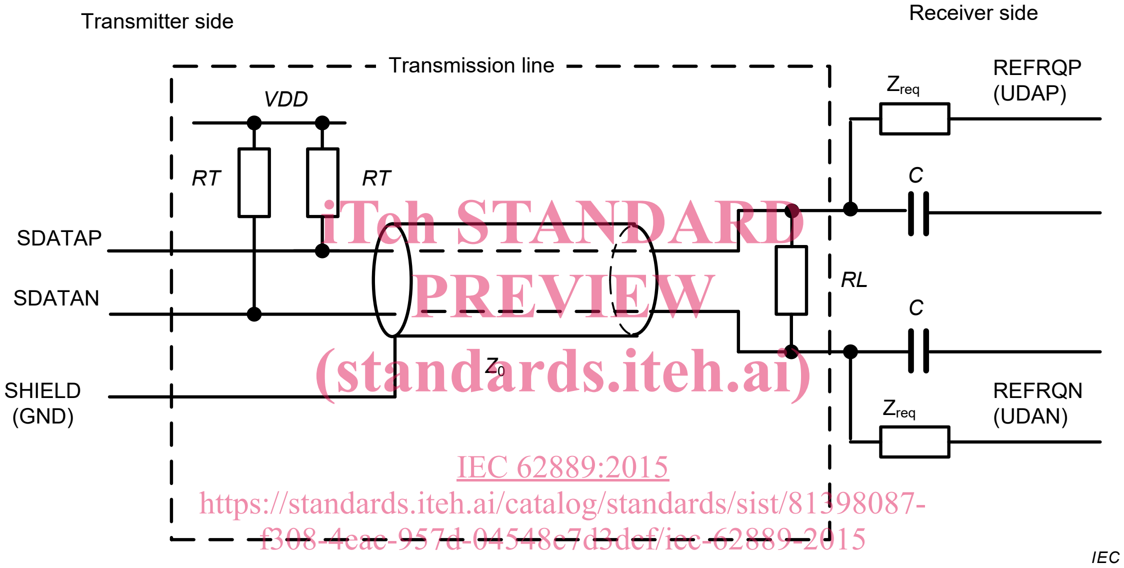
LVDS Low Voltage Differential Signaling

MSB Most Significant Bit

4 Architecture

Figure 1 illustrates the architecture of the GVIF. The fundamental operation of the GVIF is a simultaneous bi-directional data transmission technology, in which the low voltage differential signal is transmitted down from the transmitter side to the receiver side, and the common-mode voltage signal is transmitted up from the receiver side to the transmitter side through a shielded twisted differential pair cable.

The shielded twisted pair transmission line has the characteristic impedance Z_0 (see Figure 10), the line is terminated to *VDD* by *RT* of (50 ± 15) Ω on the transmitter side, and is terminated carrying differential data in *RL* of (100 ± 5) Ω on the receiver side.



where

RT are the pull-up terminated load resistors on the transmitter side (50 ± 15) Ω;

Z_0 is the characteristic impedance of the shielded twisted pair transmission line;

RL is the terminated resistor between differential data lines on the receiver side (100 ± 5) Ω;

C are AC coupling capacitors.

SDATAP/SDATAN are the down-stream positive and negative phases side signals carrying differential serial data.

REFRQP (UDAP)/REFRQN (UDAN) is the up-stream REFREQ common-mode current signal or UDA common-mode current user defined data signal. UDAP/UDAN are optional.

SHIELD (GND) is the GND and shielded ground for cable.

Z_{req} is a blocking filter for the up-stream signal. It can use resistors or inductors depending on the system implementation.

Figure 1 – Architecture of the GVIF

5 Electrical characteristics

5.1 DC electrical specifications

The DC electrical specifications of the transmitter side are shown in Table 1, and the DC electrical specifications of the receiver side are shown in Table 2.

Table 1 – DC electrical specifications of the transmitter

	Differential output peak to peak voltage (SDATAP/N) mV	Common mode voltage (SDATAP/N) V		Input REFRQ assert current (SDATAP/N) mA	Input REFRQ de-assert current (SDATAP/N) mA
	Condition: *RT* = 50 Ω *RL* = 100 Ω	Condition: *RT* = 50 Ω *RL* = 100 Ω *IRQ* = 0 mA	Condition: *RT* = 50 Ω *RL* = 100 Ω *IRQ* = 11 mA		
Minimum	690	*VDD* −0,55	*VDD* −1,2		−2,0
Typical	800				
Maximum	910	*VDD* −0,35	*VDD* −0,8	−7,3	

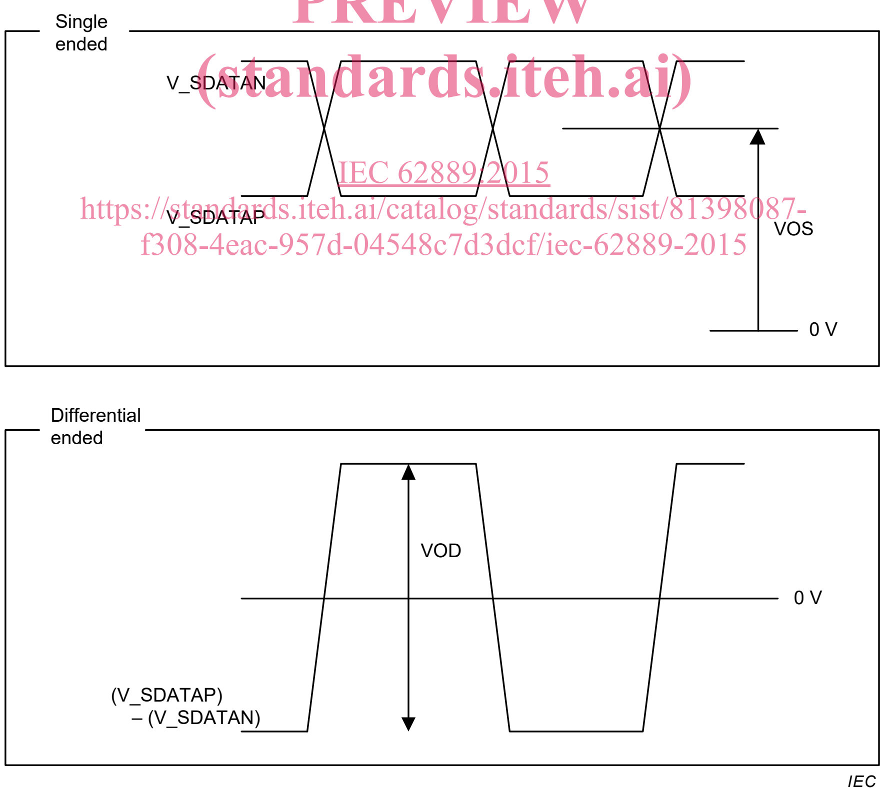


Figure 2 – VOD, VOS diagram

Table 2 – DC electrical specifications of the receiver

	Output HIGH current (REFRQP/N) mA	Output LOW current (REFRQP/N) mA
Minimum	−0,1	7,4
Maximum	0,1	11

5.2 AC electrical specifications

The AC electrical specifications of the transmitter side are shown in Table 3 and Figure 3 shows a transmitter end point eye specification (TP1). The AC electrical specifications of the receiver side are shown in Table 4.

Table 3 – AC electrical specifications of the transmitter

	SFTCLK frequency MHz	UDA data rate (up-stream) Mbit/s	SFTCLK duty factor %
Minimum	7,6	0,01	40
Maximum	160	2,41	60

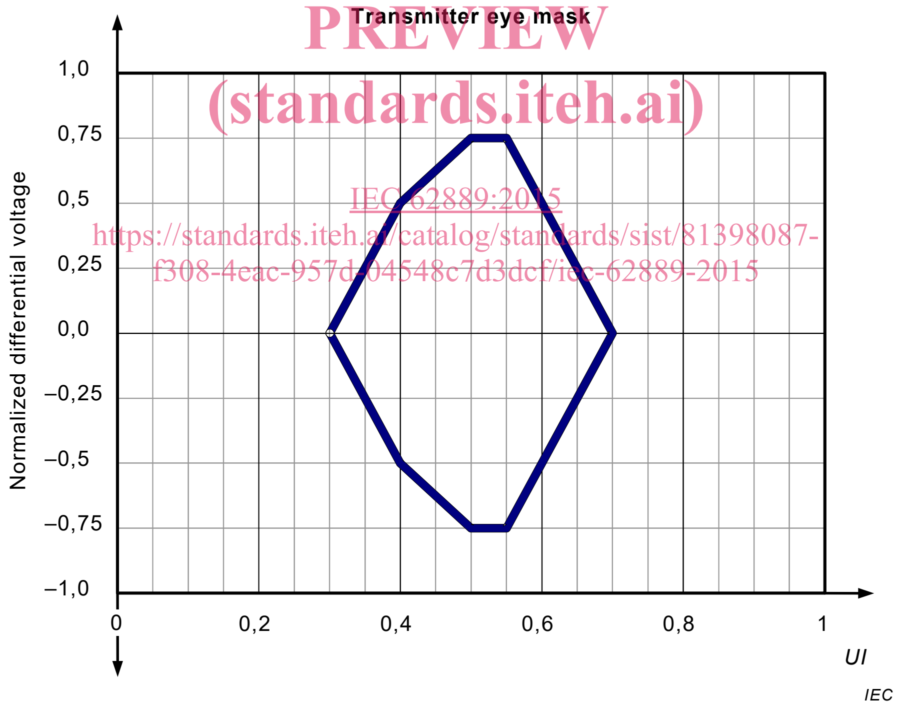


Figure 3 – Transmitter eye mask specifications (TP1)

Table 4 – AC electrical specifications of the receiver

	SFTCLK frequency MHz	UDA data rate (up-stream) Mbit/s
Minimum	7,6	0,01
Maximum	160	2,41

6 Front-end

6.1 General

The front-end block diagram of GVIF is shown in Figure 4.

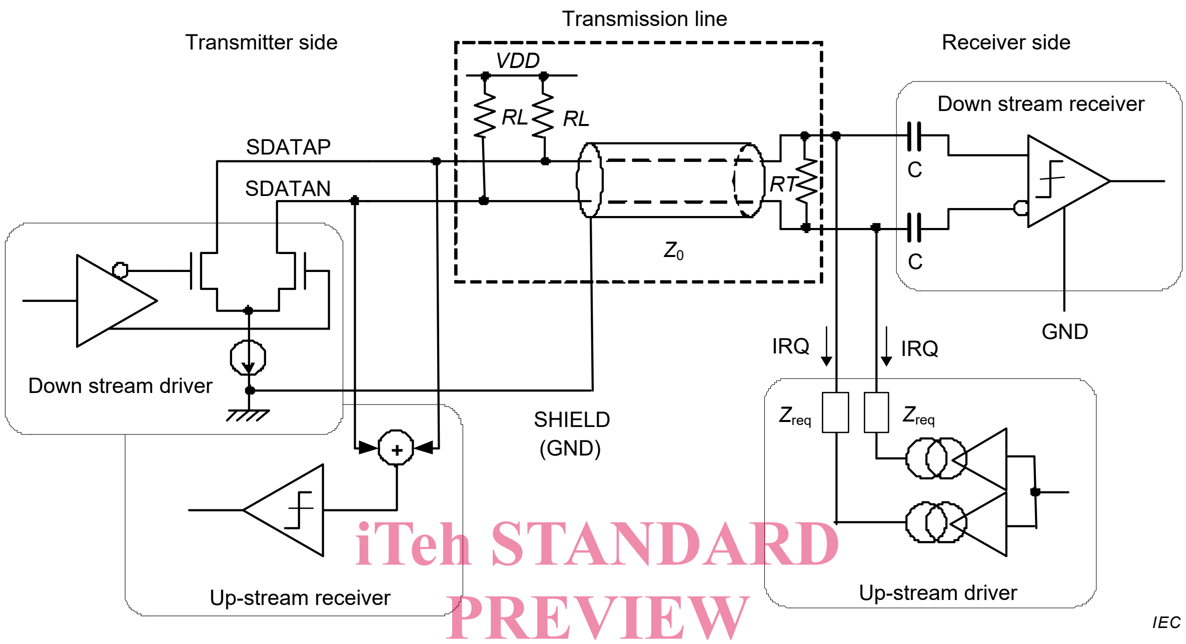


Figure 4 – Front-end block diagram

6.2 TX front-end

The TX front-end consists of a termination circuit, a down-stream driver and an up-stream receiver. The termination circuit consists of 2 resistors RL, and the SDATAP/N differential signal is pulled up to voltage reference (VDD) with a (50 ± 15) Ω resistor. The down-stream driver consists of a differential current output circuit that is driven by the serial signal from the encoder. The up-stream receiver detects the common-mode signal which RX sends through the shielded twisted pair line. The input to the down-stream driver has two modes. One is the serialized actual encoded video data input mode and the other is the reference clock signal for REFREQ hand-shake input mode. These two modes activate depending on the common-mode signal level. The common-mode signal level is normally high. When a long low level pulse is detected, the up-stream receiver activates the REFREQ signal, and changes a mode of the encoder into the reference clock mode. In case of the optional up-stream user data transmission, the up-stream receiver outputs the common-mode voltage as an UDA signal by using binary digital data sent to the encoder. In this case, the upper limit of the low pulse time is 100 µs.

6.3 RX front-end

The Rx front-end consists of AC capacitors, a termination resistor *RT* (100 ± 5) Ω, a down-stream receiver and an up-stream driver. The down-stream receiver consists of a differential input detection circuit which receives the transmission potential differential signal through the shielded twisted pair line. The up-stream driver drives the up-stream transmission signal applying a current through the termination resistor Rx through the shielded twisted pair transmission line. (A recommended transmission system and transmission line for electrical characteristics is specified in Clause 5.)