IEC 62271-101

Edition 2.0 2017-11

INTERNATIONAL STANDARD

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AMENDMENT 1
AMENDEMENT 1

High-voltage switchgear and controlgear – Part 101: Synthetic testing

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Appareillage à haute tension – Partie 101: Essais synthétiques

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IEC 62271-101:2012-10/AMD1:2017-11(en-fr)

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FOREWORD

This amendment has been prepared by subcommittee 17A: Switching devices, of IEC technical committee 17: High-voltage switchgear and controlgear.

The text of this amendment is based on the following documents:

FDIS	Report on voting
17A/1149/FDIS	17A/1154/RVD

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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The contents of the corrigendum of January 2018 have been included in this copy.

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INTRODUCTION to the Amendment

This amendment includes the following significant technical changes:

– the test procedure for test-duty T100a has been aligned with IEC 62271-100;
– Annexes A through D have been transferred to IEC 62271-306;
– Annex I has been revised and now includes Annex P of IEC 62271-100;
– Annexes K, L and N have been revised.

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2 Normative references

Replace the existing reference to IEC 62271-100:2008 by the following new reference:

IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating current circuit-breakers*

IEC 62271-100:2008/AMD 1:2012
IEC 62271-100:2008/AMD 2:2017

3.17
minimum clearing time
Replace the entire term, definition, note and source as follows:

3.17
(void)

Add, after the definition 3.18, a new term and definition as follows:

3.19
intermediate asymmetry
level of asymmetry in the other two phases having a reduced (intermediate) level of asymmetry when in a three-phase system the short-circuit current is initiated simultaneously in all phases and maximum asymmetry is obtained in one of the phases

4.1.2 High-current interval

Replace the entire subclause by the following:

The tolerance on the amplitude and the power frequency of the prospective breaking current is given in 6.103.2 and 6.104.3 of IEC 62271-100:2008. Therefore, the following conditions concerning the actual current through the test circuit-breaker shall be met:

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– for symmetrical testing the current amplitude and final loop duration shall not be less than 90 % of the required values based on the current of the test-duty considered;
– for SLF test-duties and T100s and T100a when tested with ITRV, the product of the current amplitude and the duration of the final loop shall not be less than 95 % of the required values based on the current of the test-duty considered;
– for asymmetrical testing, both the current amplitude and final loop duration shall be between 90 % and 110 % of the required values, based on the current of the test-duty considered and time constant (see Tables L.12 to L.17).

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In rare cases, where the applied voltage from the high current source is of the same magnitude as the required test voltage in a direct test circuit, a higher deviation of the last current loop is accepted provided that the prospective current loop with the auxiliary circuit-breaker arcing is within the specified tolerances.

4.1.4 High-voltage interval

Replace the first sentence of the first hyphen by the following:

The initial value of the power-frequency recovery voltage, excluding the transient oscillations, shall not be less than the equivalent initial value of the power-frequency recovery voltage specified in 6.104.7 of IEC 62271-100:2008 which, for a test with symmetrical current, starts with a minimum peak value of $0{,}95 \times k_{pp} \times U_r \sqrt{(2/3)}$.

4.2.1 Current injection methods

Replace, in the first sentence, "(see Annex B)" *by* "(see IEC 62271-306)".

Add, after the second indent, the following new sentences:

Current injection method is mandatory for:

– short-line fault test duties;

– T100s and T100a when tested with ITRV.

The time during which the arc is fed only by the injected current shall be treated as part of the length of the final current loop.

Replace the paragraph below the second hyphen by the following:

If any device with breaking capability interrupts the current through the test circuit-breaker at the same time as the test circuit-breaker, the method is not a valid current injection method.

Replace, in item c), "(see Annex B)*" by "*(see IEC 62271-306)*".*

4.2.2 Voltage injection method

Replace, in the first sentence, "(see also Annex C)*" by "*(see IEC 62271-306)".

Delete the sentence below the third hyphen of the first list.

4.2.3 Duplicate circuit method (transformer or Skeats circuit)

Replace, in the first sentence, "(see also Annex D)" *by* "(see IEC 62271-306)".

Delete the penultimate paragraph.

*Replace, in the last paragraph, "*See Annex D" *by* "See IEC 62271-306".

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4.2.4 Other synthetic test methods

Remove the last two paragraphs.

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Table 3 – Test parameters during three-phase interruption for test-duties T10, T30, T60 and T100s, k_{pp} = 1,3

*Replace "*98*" by "*97*" (3 instances).*

5.2.2 Test circuit

Replace the second sentence of the first paragraph by the following:

Examples of circuits showing voltage and current wave shapes are given in Figures 5 and 6 for single-phase and Figure 7 for three-phase.

6 Specific requirements for synthetic tests for making and breaking performance related to the requirements of 6.102 through 6.111 of IEC 62271-100:2008

Replace the existing title by the following new title:

6 Type tests

Add, before the existing text of this clause, the following new title:

6.1 General

Replace the second paragraph by the following new paragraphs and new table:

Requirements concerning testing of metal enclosed and dead tank circuit-breakers are given in Annex N.

General requirements for circuit-breakers with opening resistors are given in Annex R of IEC 62271-100:2008/AMD1:2012. A method available for testing circuit-breakers having opening resistors is reported in Annex F.

The abbreviations given in Table 6 are used to specify the operations to be performed.

Table 6 – Abbreviations used for operation during synthetic tests

Cd	Closing operation in a direct circuit at the voltage of the current source which can be less than the voltage specified in 6.104.1 of IEC 62271-100:2008
(Cd)	Closing operation as Cd, which may be carried out under no-load conditions
Cd_{asy}	Closing operation against the rated short-circuit making current according to 6.104.2 of IEC 62271-100:2008/AMD2:2017 in a direct circuit at conditions described under Cd
Cs_{sym}	Closing operation against a symmetrical current equal to the rated short-circuit breaking current, carried out at the required applied voltage in a synthetic circuit
Od	Breaking operation at the voltage of the current source only and with the specified breaking current
Os	Breaking operation with specified parameters in a synthetic circuit
t	Time interval between operations (0,3 s or 3 min depending on the rated operating sequence)
t'	Time interval between operations (3 min)
t"	Time interval between operations (15 s)
SP	Single-phase test as defined in 6.108 of IEC 62271-100:2008/AMD2:2017
DEF	Double-earth fault test as defined in 6.108 of IEC 62271-100:2008/AMD2:2017
NOTE Due to the characteristics of synthetic testing it may be difficult to comply with the specified time intervals of the rated operating sequence. See 6.105.1 of IEC 62271-100:2008/AMD1:2008.	

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In order to comply with all test requirements, it may be necessary to make more operations than specified in the normal test-duty. In such cases the circuit-breaker may be reconditioned and the test duty repeated.

6.102.10 Demonstration of arcing times

Replace the subclause by the following:

6.102.10 Demonstration of arcing times

6.102.10.1 General

The basic requirements to be met are given in 6.102.10 of IEC 62271-100:2008/AMD2:2017.

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special re-ignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. See Annex H for re-ignition methods to prolong arcing.

The "step-by-step" method described in Annex H is the method used on most synthetic tests. The method is considered to be a sufficiently close approximation of the direct testing procedure.

The arcing is prolonged by means of thermal re-ignitions. As this method makes it possible to force the test circuit-breaker to re-ignite in all conditions, special care shall be taken not to re-ignite the circuit-breaker at the instant of a current zero when the circuit-breaker can clear. For this purpose it is necessary to determine, for each terminal fault, short-line fault and out-

of-phase test duty, the minimum arcing time of the circuit-breaker. At least two breaking tests, one clearance and one re-ignition, are necessary for this determination.

The clearance at the minimum arcing time is the first valid breaking operation. The other test is performed to demonstrate that a re-ignition at an early current zero would take place between the arcing contacts. This re-ignition test shall not be the last in a test duty.

For Od operations, a tolerance of ±2 ms on the arcing time applies.

The extra tests necessary to demonstrate correct behaviour at early current zeros will usually contribute insignificantly to contact wear, etc., due to the short arcing times. Therefore, no re-conditioning should be necessary because of these tests.

The re-ignition(s) obtained when determining the minimum arcing time do(es) not indicate a failure of the circuit-breaker. However, it is important to establish that this re-ignition has taken place between the arcing contacts only. When using a current injection method, the interruption of the injected current a few loops after the re-ignition is often a useful means for the judgement. Thorough inspection of screens, arcing and main contacts, etc., should also be made to verify correct behaviour.

NOTE When performing Od-COs, or COd-COs operations the first opening operation is performed in a direct test circuit. This first opening operation should represent the minimum arcing time found for single opening operations. In case the arcing time of this first opening operation is longer than required, the test is considered as more severe.

The minimum clearing time for test-duty T100a is validated by the minimum arcing time of an interruption after a major loop with intermediate asymmetry.

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6.102.10.2 Three-phase tests

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Depending on the test circuit used, the test procedures given here may not cover the conditions of the 3rd pole-to-clear for solidly earthed systems (k_{pp} = 1,3). For this case the same procedures may be applied, with the manufacturer's consent, by combining the TRV and di/dt parameters for the 2nd pole-to-clear and the arcing time corresponding to the 3rd pole-to-clear. Alternatively, an additional test may be performed with the TRV, di/dt and the maximum arcing time corresponding to the 3rd pole-to-clear.

For alternative testing procedures of multi-enclosure type circuit-breakers with operating mechanism characteristics that require three-phase current, see Annex K.

6.102.10.2.1 Test duties T10, T30, T60, T100s, T100s(b)

The test procedure is as follows:

For convenience of testing, the pole in phase A is kept as the first-pole-to-clear.

First the minimum arcing time and correct re-ignition behaviour are established. This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times). After having done so, the setting of the control of the tripping impulse has to be advanced by approximately 40°, starting from the shortest arcing time at which the circuit-breaker cleared. For the last test, the setting of the control of the tripping impulse has to be advanced by approximately 20°, starting from the shortest arcing time at which the circuit-breaker cleared:

– first valid breaking operation: $t_{arc\ min}$, minimum arcing time in phase A;
– re-ignition test: $t_{arc\ reig} = t_{arc\ min} - 18°$, re-ignition in phase A;
– second valid breaking operation: $t_{arc\ max} = t_{arc\ min} + 40°$, longest arcing time in phase A;
– third valid breaking operation: $t_{arc\ med} = t_{arc\ min} + 20°$, medium arcing time in phase A.

The first valid breaking operation and re-ignition test consist of single opening operations. The second and third valid breaking operations are carried out as part of the rated operating sequence. If the rated operating sequence is CO-15s-CO, the third valid breaking operation is not required (see 6.102.10 of IEC 62271-100:2008/AMD2:2017).

For comparison with the arcing time settings used in three-phase direct tests, see Figure 8.

6.102.10.2.2 Test duty T100a

The intention is to demonstrate in a series of breaking tests the requirement a) and b) as defined in clause 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017:

– condition a) where arc extinction occurs in the first-pole-to-clear at the end of a major loop in the first phase with the required asymmetry criteria and with the longest possible arcing time t_{arc1};
– condition b) where arc extinction occurs at the end of an extended major loop in the last-pole-to-clear or in the second-pole-to-clear with the required asymmetry criteria and with the longest possible arcing time, t_{arc2} and t_{arc3} as follows:
  - the longest possible arcing time t_{arc2} applies for the last-pole-to-clear for circuit-breakers rated for k_{pp} = 1,5;
  - the longest possible arcing time t_{arc3} applies for the second-pole-to-clear for circuit-breakers rated for k_{pp} = 1,3 or 1,2.

The test procedure, for three-phase testing, is as follows:

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In order to simplify the test procedure, the pole in phase A is kept as the first-pole-to-clear. As a consequence the pole in phase C will be subjected to increased electrical wear. In order to obtain similar electrical wear on the poles of phase B and C, the test can be performed by exchanging the poles of phases B and C for the second breaking operation.

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First the minimum arcing time $t_{arc\ min}$ (Figures 9 and 10, first test) and re-ignition behaviour (Figures 9 and 10, second test) shall be demonstrated having intermediate asymmetry in phase A (Tables L.12 to L.17, columns 7, 8 and 9) and with the major extended loop occurring in phase C. This is done by changing the setting of the tripping impulse in steps of dα = 18° (possibly this has to be repeated several times).

Before the next operation, initiation of short-circuit current shall be advanced by 60° where the required asymmetry changes to phase A (Figures 9 and 10 third test). Arc extinction shall occur in phase A, the first-pole-to-clear at the end of a major loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition a) mentioned above.

The maximum arcing time t_{arc1} for the first pole-to-clear is achieved when the following condition is met:

$$t_{arc1} = t_{arc\ min} + \Delta t_{a1} - T \times d\alpha/360°$$

In the next operation, the initiation of short-circuit current shall be delayed by 60°. As a result the required asymmetry changes to phase C. Arc extinction shall occur in phase C at the end of a major extended loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition b) mentioned above:

– the maximum arcing time t_{arc2} for the last-pole-to-clear for circuit-breakers intended to be used in non-effectively earthed neutral systems (Figure 9 fourth test) is achieved when the following condition is met:

$$t_{arc2} = t_{arc\ min} + \Delta t_{a2} - T \times d\alpha/360°$$

– the maximum arcing time t_{arc3} for the second-pole-to-clear for circuit-breakers intended to be used in effectively earthed neutral systems (Figure 10 fourth test) is achieved when the following condition is met:

$$t_{arc3} = t_{arc\ min} + \Delta t_{a3} - T \times d\alpha/360°$$

where Δt_{a1}, Δt_{a2}, Δt_{a3} are the relevant time parameters to be selected from Tables L.12 to L.17.

The order of the last two breaking operations can be interchanged.

Some circuit-breakers will not clear at the end of a major loop after the required arcing time. However, this test is valid if the circuit-breaker clears the subsequent minor loop, that becomes the last-pole-to-clear. The corresponding parameters for the last-pole-to-clear shall be applied.

For comparison with the arcing settings used in three-phase direct tests, see Figures 9 and 10.

6.102.10.3 Single-phase tests in substitution for three-phase conditions, out-of-phase and short-line fault tests

6.102.10.3.1 General

The procedures as described in 6.102.10.3 of IEC 62271-100:2008/AMD2:2017 are applicable with the following changes. These procedures are meant to demonstrate the first-pole-to-clear, the second-pole-to-clear and the third-pole-to-clear conditions, with current and voltage parameters applicable for the first-pole-to-clear.

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6.102.10.3.3 Test-duty T100a

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The test procedure is as follows.

The minimum arcing time $t_{arc\ min}$ and re-ignition behaviour shall be demonstrated with the major loop at intermediate asymmetry (Tables L.12 to L.17, columns 8 and 9). This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times).

After that, two breaking operations at required asymmetry shall be performed as described below. Tables L.12 to L.17, columns 3 and 4, give the required values of the peak short-circuit current and loop duration that shall be attained in the last loop prior to the interruption.

One breaking operation, corresponding to condition a) of 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017, shall demonstrate interruption at the end of the major loop with an arcing time equivalent to the maximum arcing time under three-phase conditions t_{arc1} of the first-pole-to-clear.

The maximum arcing time t_{arc1} for the first pole-to-clear is achieved when the following condition is met:

$$t_{arc1} = t_{arc\ min} + \Delta t_{a1} - T \times d\alpha/360°$$

Another breaking operation, corresponding to condition b) of 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017, shall demonstrate interruption at the end of the major loop with an arcing time equivalent to the maximum arcing time under three-phase conditions:

– the maximum arcing time t_{arc2} for the last-pole-to-clear for circuit-breakers intended to be used in non-effectively earthed neutral systems (k_{pp} = 1,5) is achieved when the following condition is met:

$$t_{arc2} = t_{arc\ min} + \Delta t_{a2} - T \times d\alpha/360°$$

– the maximum arcing time t_{arc3} for the second-pole-to-clear for circuit-breakers intended to be used in effectively earthed neutral systems (k_{pp} = 1,3 or k_{pp} = 1,2) is achieved when the following condition is met:

$$t_{arc3} = t_{arc\ min} + \Delta t_{a3} - T \times d\alpha/360°$$

where Δt_{a1}, Δt_{a2}, Δt_{a3} are the relevant time parameters to be selected from Tables L.12 to L.17.

The order of the last two breaking operations may be interchanged.

Since some circuit-breakers will not clear after a major loop, a test is still valid if the circuit-breaker interrupts at the subsequent minor loop.

6.102.10.3.5 Splitting of test-duties in test series, taking into account the associated TRV for each pole-to-clear

The procedures as described in 6.102.10.3.5 of IEC 62271-100:2008/AMD2:2017 are applicable and the test procedure for synthetic testing is given in Annex L.

6.102.10.3.101 Modified procedure in cases where the circuit-breaker did not interrupt during a test with a medium arcing time, during breaking tests with symmetrical current

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If the circuit-breaker did not interrupt at the expected current zero during a breaking operation with symmetrical current with a medium arcing time then it is necessary to perform an additional breaking operation.

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The breaking operation shall demonstrate interruption with the "ultimate maximum arcing time" $t_{arc\ ult\ max}$ which is:

$$t_{arc\ ult\ max} = t_{arc\ med} + T \times (150 / 360), \text{ if } k_{pp} = 1,5$$

$$t_{arc\ ult\ max} = t_{arc\ med} + T \times (180 / 360), \text{ if } k_{pp} = 1,3,\ 1,2 \text{ or } 1,0$$

where

$t_{arc\ med}$ is the medium arcing time at which the circuit-breaker did not interrupt;

$t_{arc\ ult\ max}$ is the ultimate maximum arcing time.

If the circuit-breaker does not interrupt during this additional breaking operation, it is permissible to carry out maintenance work on the circuit-breaker according to 6.102.9.5 of IEC 62271-100:2008/AMD2:2017 and repeat the test-duty where the breaking operation with the medium arcing time is replaced by the breaking operation with the ultimate maximum arcing time.

For test duties T10, T30, T60, L_{90}, L_{75} and L_{60}, the $t_{arc\ ult\ max}$ is demonstrated with (Cd)Os.

For test duty T100s, the $t_{arc\ ult\ max}$ is demonstrated with CdOs.

For OP1 and OP2 test duties, the $t_{arc\ ult\ max}$ is demonstrated with Os.

6.106 Basic short-circuit test-duties

Delete the second paragraph and the list of abbreviations.

6.106.5 Test-duty T100a

Replace the second paragraph of item a) by the following:

Required values of the peak short-circuit current and loop duration shall be in accordance with the values in Tables L.12 to L.17.

*Delete the fourth paragraph from item a) starting with "*The required asymmetry level".

Replace the third paragraph of item b) by the following:

The corresponding corrected values can be found in Tables L.12 to L.17.

Replace the last sentence of 1) of item c) by the following:

See Annex I for more guidance.

Replace the last paragraph of 2) of item c) by the following:

Different test circuits for different asymmetry conditions may be needed in order to obtain the required values. A test with one single test circuit may over-stress the circuit-breaker and requires the consent of the manufacturer.

Add the following paragraph to item c):

3) u_c and RRRV for second-pole-to-clear and last-pole-to-clear are obtained from the respective values for symmetrical conditions reduced by the same factor as the corresponding di/dt.

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Add, at the end of the list, the following new item e):

e) Intermediate asymmetry

The phase with the intermediate asymmetry as required for testing T100a according to 6.102.10.2.2 and 6.102.10.3.3 refers to the phase, in a three-phase system, having its current zero just prior to current zero of the phase with required asymmetry. This phase also starts with a major loop of current, at current initiation. As an example the red coloured phase in tests 1 and 2 of Figures 9 and 10 (synthetic test, right hand part of the figures) fulfils this intermediate asymmetry condition.

In this particular phase, the major loops are called intermediate major loops.

The parameters of the intermediate major loop can be obtained from Tables L.12 to L.17.

6.109 Short-line fault (SLF) tests

Replace the third paragraph by the following:

The final current loop before clearing shall have an amplitude equal to the test current times $\sqrt{2}$ with a tolerance of $^{+10}_{-5}$ % including the provisions of 4.1.2.

6.111.2 General

Delete the existing title and text.

6.111.3 Characteristics of supply circuits

Replace the second paragraph by the following:

The effects of current chopping, as described in G.7, may modify the recovery voltage during the capacitive current switching tests.

Add, after the second paragraph, the following new paragraph:

A test circuit with a 50 Hz current circuit may be used to prove the capacitive current switching capability for a rating of 60 Hz, provided that the recovery voltage fulfils the 60 Hz requirements (see 6.111.3 of IEC 62271-100:2008/AMD2:2017). The setting of the contact separation should be based on the frequency of the current source.

6.111.7 Test voltage

Replace the existing text by the following:

The prospective recovery voltage during synthetic capacitive current switching tests shall be calculated based on the test voltage of the corresponding single-phase direct test, as defined in 6.111.7 of IEC 62271-100:2008/AMD2:2017, and comply with the requirements of 6.111.10 of IEC 62271-100:2008/AMD2:2017.

Due to limitations of some synthetic test circuits the following additional requirements apply to the recovery voltage:

– The peak value of the a.c. component of the recovery voltage should be kept as close as possible to $k_c \times U_r \sqrt{2}/\sqrt{3}$;

– The d.c. component of the recovery voltage shall not decay more than 10 % within an interval of 0,3 s after final arc extinction, except for test duty LC1 and/or CC1;

– The recovery voltage shall not fall below $1{,}5 \times k_c \times U_r \sqrt{2}/\sqrt{3}$ within an interval of 0,1 s after final arc extinction.

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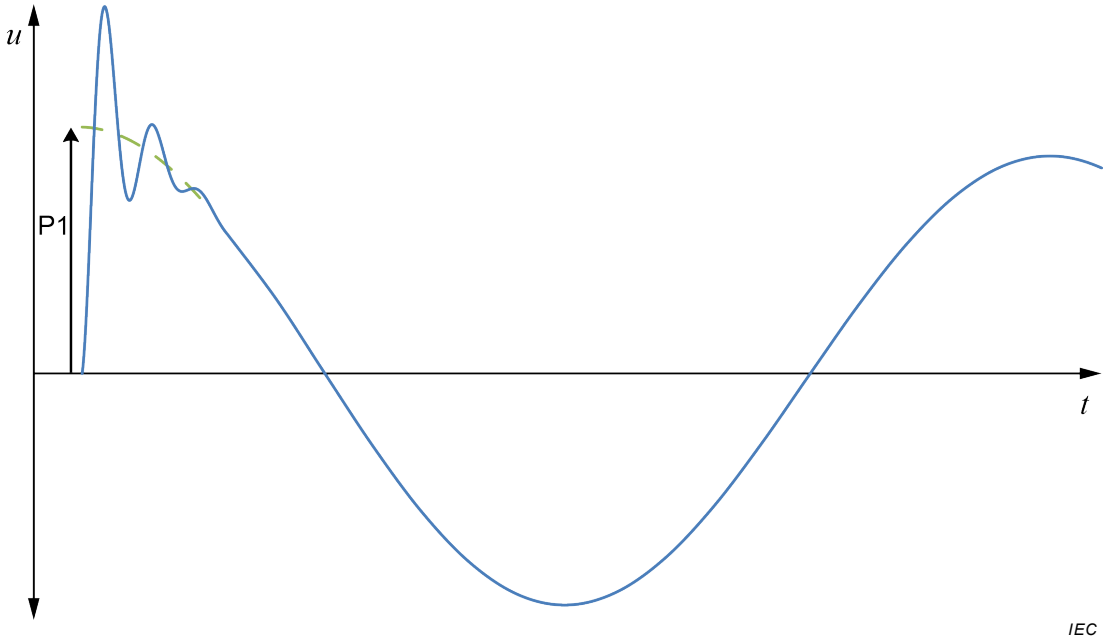
Graphical representation is shown in Figure 8.

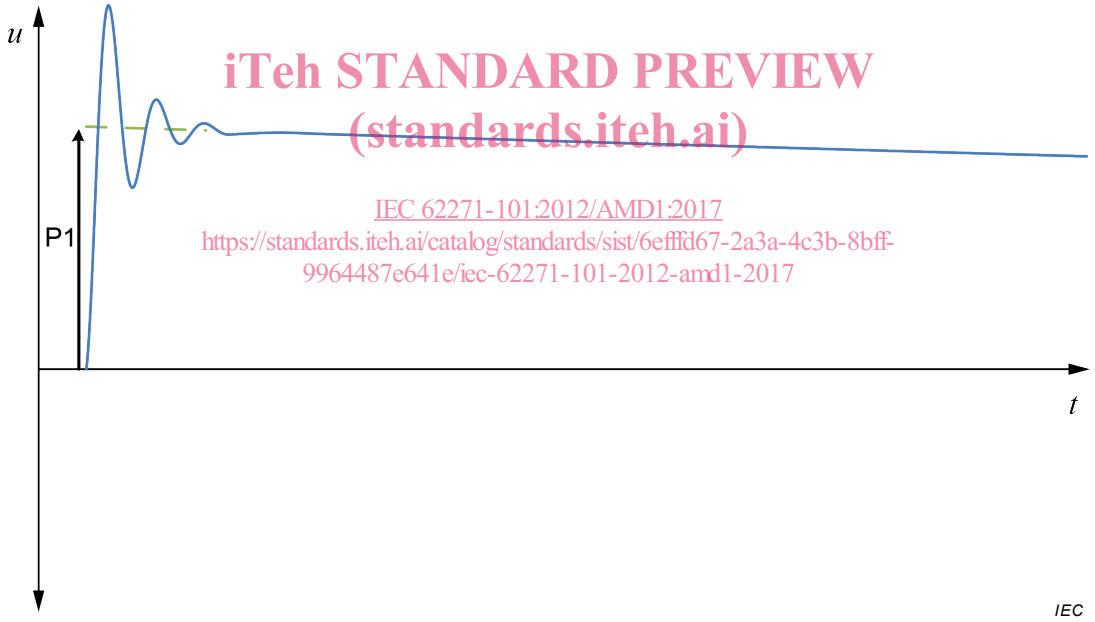
Examples of synthetic capacitive current switching circuits are given in Annex G.

Figure 2 – Examples of evaluation of recovery voltage

Replace Figure 2 by the following:



a) Example of a power-frequency recovery voltage



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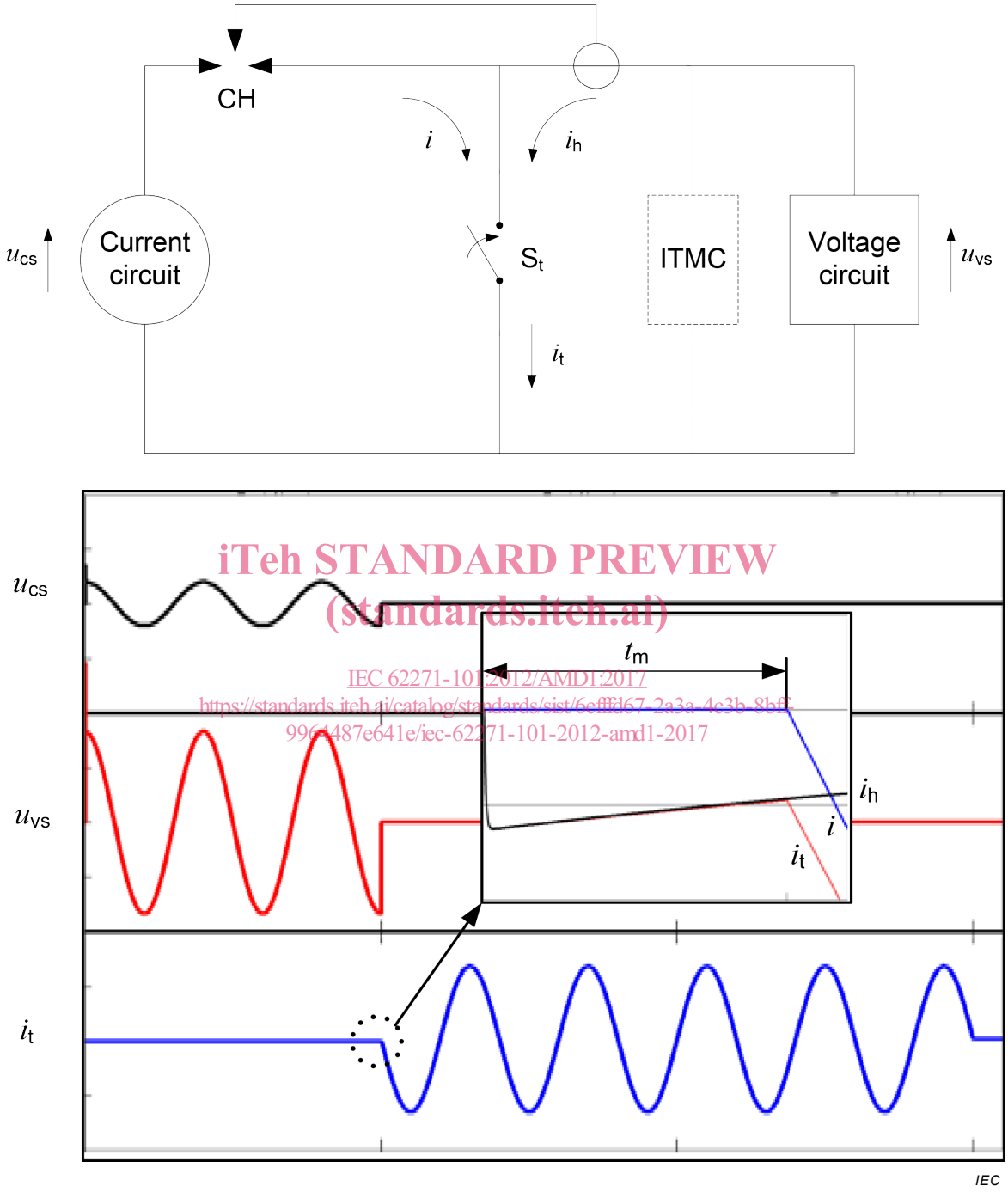
b) Example of a d.c. steady-state recovery voltage

P1	Point of initial value of (power frequency or d.c. steady-state) recovery voltage, $\geq 0{,}95 \times k_{pp} \times U_r \times \sqrt{\frac{2}{3}}$
Blue line	Tested recovery voltage
Green dotted line	Tested power frequency or d.c. steady-state recovery voltage

Figure 2 – Examples of evaluation of initial recovery voltage

Figure 5 – Typical synthetic making circuit for single-phase tests

Replace Figure 5 by the following:



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Key

u_{cs}	voltage of current circuit	u_{vs}	voltage of voltage circuit
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	t_m	time delay of making device

Figure 5 – Example of synthetic making circuit for single-phase tests