SLOVENSKI STANDARD
SIST EN 62416:2010

01-september-2010

Polprevodniški elementi - Preskušanje z vročimi nosilci pri tranzistorjih MOS (IEC 62416:2010)

Semiconductor devices - Hot carrier test on MOS transistors (IEC 62416:2010)

Halbleiterbauelemente - Hot-Carrier-Prüfverfahren für MOS-Transistoren (IEC 62416:2010)

Dispositifs à semi-conducteurs - Essai de porteur chaud sur les transistors MOS (CEI 62416:2010)

Ta slovenski standard je istoveten z: **EN 62416:2010**

ICS:

31.080.30	Tranzistorji	Transistors

SIST EN 62416:2010 **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62416

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ICS 31.080

English version

Semiconductor devices - Hot carrier test on MOS transistors

(IEC 62416:2010)

Dispositifs à semi-conducteurs - Essai de porteur chaud sur les transistors MOS
(CEI 62416:2010)

Halbleiterbauelemente - Hot-Carrier-Prüfverfahren für MOS-Transistoren
(IEC 62416:2010)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47/2041/FDIS, future edition 1 of IEC 62416, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62416 on 2010-06-01.

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The following dates were fixed:

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– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2013-06-01

Endorsement notice

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IEC 62416

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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Hot carrier test on MOS transistors

Dispositifs à semiconducteurs – Essai de porteur chaud sur les transistors MOS

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FOREWORD

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International Standard IEC 62416 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2041/FDIS	47/2048/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – HOT CARRIER TEST ON MOS TRANSISTORS

1 Scope

This standard describes the wafer level hot carrier test on NMOS and PMOS transistors. The test is intended to determine whether the single transistors in a certain (C)MOS process meet the required hot carrier lifetime.

2 Abbreviations and letter symbols

In this document the following abbreviations and letter symbols apply:

MOS	Metal Oxide Semiconductor
NMOS	n-channel MOS transistor
PMOS	p-channel MOS transistor
(C)MOS	Complementary MOS
L [µm]	length of polysilicon gate of MOS transistor
W [µm]	width of polysilicon gate of MOS transistor
$L_{nominal}$ [µm]	minimum L allowed by the design rules of the process
$W_{nominal}$ [µm]	minimum W allowed by the design rules of the process
V_{gs} [V]	gate-source voltage of MOS transistor
V_{ds} [V]	drain-source voltage of MOS transistor
V_{bs} [V]	backgate-source voltage of MOS transistor
I_{ds} [µA]:	drain-source current of MOS transistor
I_b [µA]	substrate current of MOS transistor
I_g [nA]	gate current of MOS transistor
$V_{gs,stress}$ [V]	V_{gs} biasing condition during hot carrier stress
$V_{ds,stress}$ [V]	V_{ds} biasing condition during hot carrier stress
V_{ds,use_max} [V]	maximum V_{ds} allowed by the design rules of the process as stated in the design manual
$V_{ds,breakdown}$ [V]	V_{ds} at which avalanche or punch-through currents become dominant; defined as V_{ds} at which I_{ds}= 1,5 × (I_{ds} at V_{ds,use_max}) while V_{gs}= V_{ds,use_max}
V_t [V]	threshold voltage of MOS transistor defined as V_{gs} voltage at which I_{ds}= 0,01 × W / L [µA]. Other (commonly agreed) definitions of V_t are also allowed as long as this is clearly reported.
g_m [µA/V]	transconductance of MOS transistor
$g_{m,max}$ [µA/V]	maximum transconductance of MOS transistor
$I_{ds,sat}$ [µA]	saturated drain-source current at V_{gs}= V_{ds}= $V_{ds,use\_,max}$; $I_{ds,sat\_forward}$ measured with source and drain having same polarity as during stress, $I_{ds,sat\_reverse}$ measured with source and drain polarity interchanged with respect to stress.
L(MOST)	length of the square MOS transistor (L = W)
$g_{m,max}$ (MOST)	$g_{m,max}$ of the square MOS transistor (L = W)