SLOVENSKI STANDARD
SIST EN 62374-1:2011

01-januar-2011

Nadomešča:
SIST EN 62374:2008

Polprevodniški elementi - 1. del: Preskus dielektrične plasti vrat s časovno odvisnim dielektričnim prebojem (TDDB) (IEC 62374-1:2010)

Semiconductor devices - Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers (IEC 62374-1:2010)

Halbleiterbauelemente - Teil 1: Prüfung auf zeitabhängigen dielektrischen Durchbruch (TDDB) bei Isolationsschichten zwischen metallischen Leiterbahnen (IEC 62374-1:2010)

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Dispositifs à semiconducteurs - Partie 1: Essai de rupture diélectrique en fonction du temps (TDDB) pour les couches intermétalliques (CEI 62374-1:2010)

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Ta slovenski standard je istoveten z: **EN 62374-1:2010**

ICS:

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

SIST EN 62374-1:2011 **en**

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EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62374-1

November 2010

ICS 31.080

Supersedes EN 62374:2007

English version

Semiconductor devices -
Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers
(IEC 62374-1:2010)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

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Ref. No. EN 62374-1:2010 E

SIST EN 62374-1:2011

Foreword

The text of document 47/2063/FDIS, future edition 1 of IEC 62374-1, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62374-1 on 2010-11-01.

This European Standard supersedes EN 62374:2007.

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– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2011-08-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2013-11-01

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SIST EN 62374-1:2011

IEC 62374-1

Edition 1.0 2010-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

PRICE CODE
CODE PRIX **P**

ICS 31.080

ISBN 978-2-88912-178-6

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SEMICONDUCTOR DEVICES –

Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

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International Standard IEC 62374-1 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2063/FDIS	47/2077/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62374 series, under the general title *Semiconductor devices*, can be found on the IEC website.

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SEMICONDUCTOR DEVICES –

Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

1 Scope

This part of IEC 62374 describes a test method, test structure and lifetime estimation method of the time-dependent dielectric breakdown (TDDB) test for inter-metal layers applied in semiconductor devices.

2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1
leakage current of inter-metal layer
I_{leak}
current through the dielectric layer when a use voltage is applied

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2.2
initial leakage current of inter-metal layer
I_{leak-0}
leakage current of inter-metal layer before a stress voltage is applied

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2.3
compliance current
I_{comp}
maximum current of the voltage-forcing equipment

NOTE A compliance limit can be specified for a particular test.

2.4
measured leakage current of inter-metal layer
I_{meas}
measured current in constant voltage stress (CVS) test

2.5
breakdown time
t_{bd}
summation of time during which stress voltage is applied to inter-metal layer until failure

NOTE In CVS test, applied stress voltage is interrupted by measuring and assessing repeatedly (see Figure 5).

2.6
dielectric layer thickness
t_{d}
physical thickness of dielectric layer which is pitched between metal lines

2.7
stress voltage
V_{stress}
voltage applied during CVS test

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2.8
use voltage
V_{use}
voltage applied during pre-test and used for lifetime estimation

NOTE This voltage is usually power supply voltage.

2.9
metal electrode length
L
total length of metal electrode which is pitching the dielectric layer

2.10
electric field for inter-metal layer
E_{im}
voltage across a dielectric layer divided by its horizontal width between metal lines

NOTE The dielectric layer width should be determined by a consistent documented method by the physical measurement method with SEM, TEM or other. The method or a reference to a documented standard which describes the method should be included in the data report.

3 Test equipment

This TDDB test can be applied by both the package level test and the wafer level test. A high temperature oven is used for the package level test. In the case of the wafer level test, a wafer probe with a hot plate or hot chuck is necessary. Additionally the instruments need to have sufficient resolution to detect changes of leakage current under high temperature condition.

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NOTE Package level test is test on test structures assembled in package.

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4 Test samples

4.1 General

Test samples for TDDB test for inter-metal layer shall have the following test structure.

4.2 Test structure

An appropriate test structure for this test is an interdigitated one as shown in Figure 1, consisting of comb and serpent patterns, which are connected to the voltage source lines. There is an alternative structure, that is the interdigitated comb and comb structure shown in Figure 2. Test structure leads shall be designed to prevent unexpected failures outside the test structure during the TDDB test. Patterns with vias (Figures 3 and 4) need to be considered because the failure mechanism might be different from a line-to-line pattern without via. Unless otherwise specified comb and serpent pattern are be recommended. The minimum line-to-line spacing is the most severe condition for this mechanism. Therefore, the minimum dimension allowed by the layout rule shall be evaluated. The total length of the metal line is recommended to be in the range from 0,01 m to 1 m. For the accurate lifetime estimation, it is recommended that at least three device conditions of area or length be used, so proper scaling can be achieved. Unless otherwise specified the above-mentioned conditions shall be used for test structure parameters.

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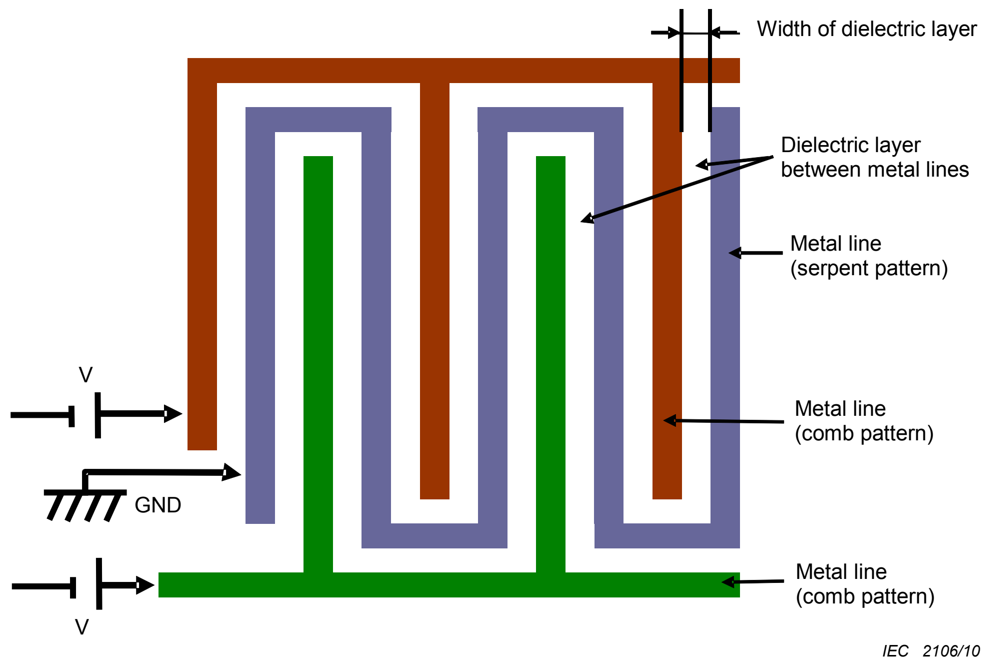

Figure 1 – Schematic image of test structure (comb and serpent pattern)

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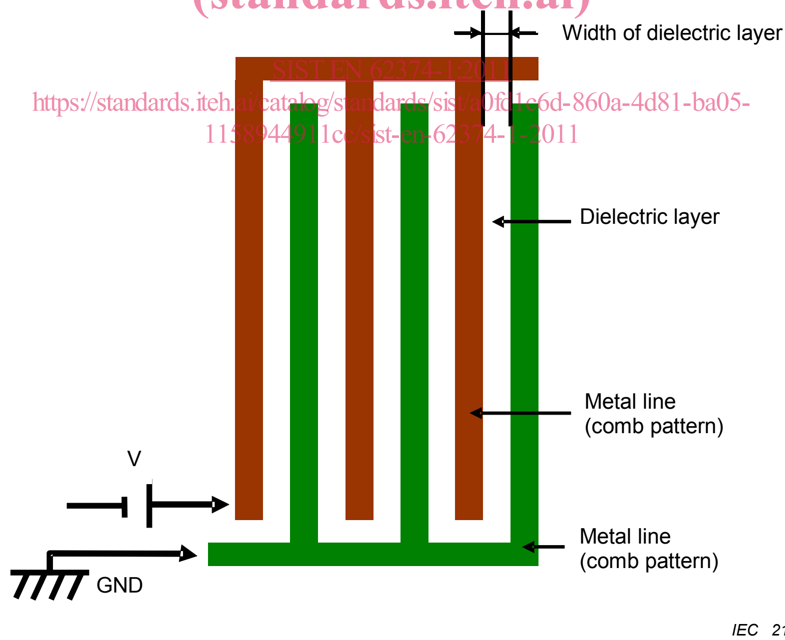

Figure 2 – Schematic image of test structure (comb and comb pattern)