SLOVENSKI STANDARD
SIST EN 60191-6:2010

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Nadomeġļa:
SIST EN 60191-6:2005

Standardizacija mehanskih lastnosti polprevodniġkih elementov - 6. del: Sploġna pravila za pripravo tehniļnih risb okrovov povrġinsko nameġļenih polprevodniġkih elementov (IEC 60191-6:2009)

Mechanical standardization of semiconductor devices -- Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages (IEC 60191-6:2009)

Mechanische Normung von Halbleiterbauelementen - Teil 6: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen (IEC 60191-6:2009)

Normalisation mécanique des dispositifs à semi-conducteurs - Partie 6: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semi-conducteurs pour montage en surface (CEI 60191-6:2009)

Ta slovenski standard je istoveten z: **EN 60191-6:2009**

ICS:

01.100.25	Risbe s podroļja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

SIST EN 60191-6:2010 **en,fr**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60191-6

December 2009

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Supersedes EN 60191-6:2004

English version

Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

(IEC 60191-6:2009)

Normalisation mécanique des dispositifs à semi-conducteurs - Partie 6: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semi-conducteurs pour montage en surface (CEI 60191-6:2009)

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This European Standard was approved by CENELEC on 2009-12-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: Avenue Marnix 17, B - 1000 Brussels

Ref. No. EN 60191-6:2009 E

Foreword

The text of document 47D/736/CDV, future edition 3 of IEC 60191-6, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6 on 2009-12-01.

This European Standard supersedes EN 60191-6:2004.

EN 60191-6:2009 includes the following significant changes with respect to EN 60191-6:2004:

– scope is modified to cover all surface-mounted devices discrete semiconductors with lead count of greater or equal to 8;

– editorial modifications on several pages; and

– technical revision to ball grid array package (BGA) especially its geometrical drawing format. (two types of BGA would unify as one type as a result of revising drawing format.)

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2010-09-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2012-12-01

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6:2009 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60191-3	NOTE	Harmonized as EN 60191-3:1999 (not modified).
ISO 2692	NOTE	Harmonized as EN ISO 2692:2006 (not modified).

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-1	2007	Mechanical standardization of semiconductor devices - Part 1: General rules for the preparation of outline drawings of discrete devices	EN 60191-1	2007
IEC 60191-4 A1 A2	1999 2001 2002	Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4 A1 A2	1999 2002 2002
ISO 1101	2004	Geometrical Product Specifications (GPS) - Geometrical tolerancing - Tolerances of form, orientation, location and run-out	EN ISO 1101	2005

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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

Normalisation mécanique des dispositifs à semi-conducteurs – Partie 6: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semi-conducteurs pour montage en surface

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CONTENTS

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 60191-6 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition of IEC 60191-6 cancels and replaces the second edition, published in 2004 and constitutes a technical revision. This edition includes the following significant changes with respect to the previous edition:

a) scope is modified to cover all surface-mounted devices discrete semiconductors with lead count of greater or equal to 8;
b) editorial modifications on several pages; and
c) technical revision to ball grid array package (BGA) especially its geometrical drawing format. (two types of BGA would unify as one type as a result of revising drawing format.)

The text of this standard is based on the following documents:

CDV	Report on voting
47D/736/CDV	47D/749/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of IEC 60191 series under the general title *Mechanical standardization of semiconductor devices* can be found on the IEC website.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

1 Scope

This part of IEC 60191 gives general rules for the preparation of outline drawings of surface-mounted semiconductor devices. It supplements IEC 60191-1 and IEC 60191-3. It covers all surface-mounted devices discrete semiconductors with lead count of greater or equal to 8, as well as integrated circuits classified as form E in Clause 3 of IEC 60191-4.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-1:2007, *Mechanical standardization of semiconductor devices – Part 1: General rules for the preparation of outline drawings of discrete devices*

IEC 60191-4:2002, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*

ISO 1101:2004 *Geometrical Product Specifications (GPS) – Geometrical tolerancing – Tolerances of form, orientation, location and run-out*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
seating plane
plane which designates the plane of contact of the package, including any stand-off, with the surface on which it will be mounted

NOTE This plane is often used as the reference plane.

3.2
reference plane
plane parallel to the seating plane at a distance A3 above seating plane (does not apply to leadless package)

NOTE 1 The distance A3 is known as the reference plane distance. It determines the terminal projection zone (see Figure 1).

NOTE 2 This distance is a theoretical dimension which is not related to any feature of the package. Its value is chosen for each package so the length of terminal projection zone L_p is a good approximation of the terminal length used for mounting, e.g. the length of the part of the terminal that is soldered to the substrate.

3.3
terminal position area
maximum area on the seating plane within which the terminal projection zone is located, taking into account the maximum values of L_p and b_p

NOTE 1 The surface of the terminal position area is equal to $l_1 \times b_3$ with, generally

$$l_1 = L_p \text{ max.} + (\text{HDmax.} - \text{HDmin.})/2$$

$$= L_p \text{ max.} + (\text{HEmax.} - \text{HEmin.})/2$$

$$\text{and } b_3 = b_p \text{ max.} + x$$

NOTE 2 Checking can be carried out by means of an appropriate gauge (see Figure 2)

3.4
pattern of terminal position areas
group of all terminal position areas of a leaded package or folded lead package in the seating plane

NOTE 1 For a leadless package, it is the projection of its metallized pads or terminals on the seating plane.

NOTE 2 The true positions of the centres of the terminal position areas are located on a grid with a modulus

$\boxed{e} / \boxed{eD}$ or $\boxed{e} / \boxed{eE}$

NOTE 3 The pattern of terminal position areas does not include tolerances stemming from mounting substrates (printed board) design and placement machine accuracy.

3.5
coplanarity of terminals

profile tolerance controlling the location of the crowns of the bottom terminals with respect to the seating plane

NOTE In all the other cases, the requirement for coplanarity of terminals is clarified by a note.

3.6
datum
geometrical established planes for controlling the tolerance zone

NOTE Datum S should be established by seating plane.

4 Design rules

The outline drawing of a surface-mounted semiconductor device package shall comprise in the given sequence:

– the drawing (strictly speaking);
– the tables of dimensions;
– the notes to the tables and the drawings;
– the codification.

The drawing shall conform with the general rules for drawings laid down in IEC 60191-1, Clause 4 and Clause 5, as well as with the specific definitions of Clause 3 above.

The following, Clause 5 and Clause 6 give, respectively, the tables of dimensions to be specified and the notes to be called, where relevant. Supplementary dimensions and notes may be added when required.