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Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

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IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue
New York, NY 10016-5997
United States of America
stds.info@ieee.org
www.ieee.org

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QUALITY OF ELECTRONIC AND SOFTWARE INTELLECTUAL PROPERTY USED IN SYSTEM AND SYSTEM ON CHIP (SOC) DESIGNS

FOREWORD

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IEEE Standard for Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

Sponsor

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Approved 16 June 2011

IEEE-SA Standards Board

This standard contains material originally published by the VSI Alliance and currently available in the public domain (http://vsi.org/). Acknowledgment is made to the VSI Alliance, who developed the VSIA-QIP v4.0 spreadsheet and macros, and the QIP Metric Users Guide Version 4.0 document from which some material in this standard was derived.

Abstract: A standard XML format for representing electronic design intellectual property (IP) quality information, based on an information model for IP quality measurement, is defined. It includes a schema and the terms that are relevant for measuring IP quality, including the software that executes on the system. The schema and information model can be focused to represent particular categories of interest to IP users. In the context of this document, the term *IP* shall be used to mean *electronic design intellectual property.* Electronic design intellectual property is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media.

Keywords: AMS, analog and mixed signal, design environment, EDA, electronic design automation, electronic system level, ESL, IEEE 1734, implementation constraints, MEMS, microelectromechanical systems, QIP, Quality IP metrics, register transfer logic, RTL, SCRs, semantic consistency rules, use models, verification IP, VIP, XML design meta data, XML schema

IEEE Introduction

This introduction is not part of IEEE Std 1734-2011, IEEE Standard for Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs.

The purpose of this standard is to provide a unified view of quality measures for *electronic design intellectual property* (IP) to facilitate the use and integration of IP used in electronic system design. These quality measures can be evaluated in the context of the end application to help determine suitability and plan mitigation measures for potential integration gaps. This can enable the continuous improvement of IP used for system design and verification by providing a mechanism for qualitative comparison between such IP. The standard IP quality measures and characteristic exchange format defined can be incorporated into a variety of electronic design automation (EDA) tools. The goal of this specification is to specify a quality standard metric that will account for the variances in designing, verifying and testing the IP, which will result in fair quality assessment, reducing the risk of schedule slip or mask spins due to faulty IP.

The working group consisted of electronic system, IP provider, semiconductor, and EDA companies, and used the VSI Alliance Quality IP (QIP) metric as a baseline for the metrics. The data specified by the standard is extensible in locations specified in the schema. This structure can be used as the basis of both manual and automatic methodologies.

This standardization project provides electronic design and SoC engineers with a well-defined standard that meets their requirements in evaluating and validating IP and enables a step function increase in their productivity. This project also provides the EDA industry with a standard to which they can adhere and that they can support in order to deliver their solutions in this area.

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Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

1. Overview

1.1 Scope

This specification defines a standard XML format for representing electronic design intellectual property (IP) quality information, based on an information model for IP quality measurement. It includes a schema and the terms that are relevant for measuring IP quality, including the software that executes on the system. The schema and information model can be focused to represent particular categories of interest to IP users. In the context of this document, the term *IP* shall be used to mean *electronic design intellectual property*. Electronic design intellectual property is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media.

1.2 Purpose

The purpose of this standard is to provide a unified view of quality measures for IP to facilitate the use and integration of this IP used in electronic system design. This will enable the continuous improvement of IP used for system design and verification by providing a mechanism for qualitative comparison between such

IP. The standard IP quality measures and characteristic exchange format defined can be incorporated into a variety of electronic design automation (EDA) tools.

1.3 Design environment

The IP quality specification is a mechanism to express and exchange information about design IP, its development, data management, documentation, verification and validation processes, as well as evaluating the quality and stability of the owning or development organization. While the XML description formats are the core of this standard, describing the quality specification in the context of its basic use model, the design environment (DE), more readily depicts the extent and limitations of the semantic intent of the data. The DE coordinates a set of tools and IP, or expressions of that IP (e.g., models), through the evaluation and manipulation of metadata descriptions of the IP such that the IP can be efficiently integrated into and SoC and reused.

1.3.1 Design intellectual property

Quality IP (QIP) is structured around the concept of IP reuse. *Electronic design intellectual property,* or IP, is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media. The name IP is partially derived from the common practice of considering a collection of this type to be the intellectual property of one party. Both hardware and software collections are encompassed by this term.

Examples of these collections may include the following:

a) Design objects—This can include the following:
   1) Fixed HDL descriptions: Verilog®[1], VHDL
   2) Verification IP descriptions: Verilog (see IEEE Std 1364™ [B2], IEC/IEEE 61691-1-1 [B1])[2]
   3) Hardened IP descriptions: GDSII, LEF, LIB, LVS, Characterization Reports
   4) Software descriptions: C, C++, etc.
   5) HDL-specified verification IP (e.g., basic stimulus generators and checkers)

b) IP views—This is a list of different views (levels of description and/or languages) to describe the IP object. These views include the following:
   1) Design view: RTL Verilog or VHDL, flat or hierarchical components
   2) Simulation view: model views, targets, simulation directives, etc.
   3) Documentation view: standard, user guide, etc.
   4) Supporting scripts: synthesis, makefile, manufacturing test, etc.

1.4 QIP-compliant enabled implementations

Complying with the rules outlined in this subclause allows the provider of tools or IP to class their products as *QIP compliant.* Conversely, any violation of these rules removes that naming right. This subclause first

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[2] The numbers in brackets correspond to that of the bibliography in Annex A