

## SLOVENSKI STANDARD SIST EN 60191-6-20:2010

01-december-2010

Standardizacija mehanskih lastnosti polprevodniških elementov - 6-20. del: Splošna pravila za izdelavo tehničnih risb površinsko montiranih sklopov polprevodniških elementov - Merilne metode za mere majhnih okrovov s priključki v obliki črke J (SOJ) (IEC 60191-6-20:2010)

Mechanical standardization of semiconductor devices - Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Measuring methods for package dimensions of small outline J-lead packages (SOJ) (IEC 60191-6-20:2010) **Teh STANDARD PREVIEW** 

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Mechanische Normung von Halbleiterbauelementen - Teil 6-20: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Messverfahren für Gehäusemaße von kleinen Gehäusen mit J-förmigen Anschlüssen (SOJ) (IEC 60191-6-20:2010)

Normalisation mécanique des dispositifs à semiconducteurs - Part 6-20: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semiconducteurs pour montage en surface - Méthodes de mesure pour les dimensions des boîtiers à sortie en J (SOJ) de faible encombrement (CEI 60191-6-20:2010)

Ta slovenski standard je istoveten z: EN 60191-6-20:2010

#### ICS:

01.100.25 Risbe s področja Electrical and electronics

elektrotehnike in elektronike engineering drawings

31.080.01 Polprevodniški elementi Semiconductor devices in

(naprave) na splošno general

SIST EN 60191-6-20:2010 en

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EN 60191-6-20

Mechanische Normung von

Teil 6-20: Allgemeine Regeln für die

kleinen Gehäusen mit J-förmigen

Erstellung von Gehäusezeichnungen von

Halbleiterbauelementen -

SMD-Halbleitergehäusen -

(IEC 60191-6-20:2010)

NORME FUROPÉENNE **EUROPÄISCHE NORM** 

October 2010

ICS 31.080.01

English version

Mechanical standardization of semiconductor devices -Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages -Measuring methods for package dimensions of small outline J-lead packages (SOJ)

(IEC 60191-6-20:2010)

Normalisation mécanique des dispositifs à semiconducteurs -

Part 6-20: Règles générales pour la préparation des dessins d'encombrement

des boîtiers pour dispositifs à

semiconducteurs pour montage en place per plac surface -

Méthodes de mesure pour les dimensions S. ite Anschlüssen (SOJ)

des boîtiers à sortie en J (SOJ) de faible

encombrement

(CEI 60191-6-2012010) ndards.iteh.ai/catalog/standards/sist/52d1a197-bb17-4c61-84dd-

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European Committee for Electrotechnical Standardization Comité Européen de Normalisation Electrotechnique Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

#### **Foreword**

The text of document 47D/771/FDIS, future edition 1 of IEC 60191-6-20, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-20 on 2010-10-01.

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The following dates were fixed:

 latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement

(dop) 2011-07-01

 latest date by which the national standards conflicting with the EN have to be withdrawn

(dow) 2013-10-01

Annex ZA has been added by CENELEC.

### **Endorsement notice**

The text of the International Standard IEC 60191-6-20:2010 was approved by CENELEC as a European Standard without any modification. (standards.iteh.ai)

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## Annex ZA (normative)

## Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	EN/HD	<u>Year</u>
IEC 60191-4	-	Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4	-
IEC 60191-6	iTe	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages		-

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IEC 60191-6-20

Edition 1.0 2010-08

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE

Mechanical standardization of semiconductor devices — W Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages — Measuring methods for package dimensions of small outline J-lead packages (SOJ)

https://standards.iteh.ai/catalog/standards/sist/52d1a197-bb17-4c61-84dd-

Normalisation mécanique des dispositifs à semiconducteurs – Partie 6-20: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semiconducteurs pour montage en surface – Méthodes de mesure pour les dimensions des boîtiers à sortie en J (SOJ) de faible encombrement

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

### **MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES -**

Part 6-20: General rules for the preparation of outline drawings of surface mounted semiconductor device packages –

Measuring methods for package dimensions of small outline J-lead packages (SOJ)

#### **FOREWORD**

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International Standard IEC 60191-6-20 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting	
47D/771/FDIS	47D/775/RVD	

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directive, Part 2.

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A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- · reconfirmed,
- withdrawn,
- · replaced by a revised edition, or
- amended.

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