
**Standardizacija mehanskih lastnosti polprevodniških elementov - 6-21. del:
Splošna pravila za izdelavo tehničnih risb površinsko montiranih sklopov
polprevodniških elementov - Merilne metode za mere majhnih okrovov (SOP) (IEC
60191-6-21:2010)**

Mechanical standardization of semiconductor devices - Part 6-21: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Measuring methods for package dimensions of small outline packages (SOP) (IEC 60191-6-21:2010)

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Mechanische Normung von Halbleiterbauelementen - Teil 6-21: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Messverfahren für Gehäusemaße von kleinen Gehäusen (SOP) (IEC 60191-6-21:2010)

Normalisation mécanique des dispositifs à semiconducteurs - Part 6-21: Règles générales pour la préparation des dessins d'encombrement des boîtiers pour dispositifs à semiconducteurs pour montage en surface - Méthodes de mesure pour les dimensions des boîtiers de faible encombrement (SOP) (CEI 60191-6-21:2010)

Ta slovenski standard je istoveten z: EN 60191-6-21:2010

ICS:

01.100.25	Risbe s področja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

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EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 60191-6-21

October 2010

ICS 31.080.01

English version

**Mechanical standardization of semiconductor devices -
Part 6-21: General rules for the preparation of outline drawings of surface
mounted semiconductor device packages -
Measuring methods for package dimensions of small outline packages
(SOP)
(IEC 60191-6-21:2010)**

Normalisation mécanique des dispositifs à
semiconducteurs -
Part 6-21: Règles générales pour la
préparation des dessins d'encombrement
des boîtiers pour dispositifs à
semiconducteurs pour montage en
surface -
Méthodes de mesure pour les dimensions
des boîtiers de faible encombrement
(SOP)
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Mechanische Normung von
Halbleiterbauelementen -
Teil 6-21: Allgemeine Regeln für die
Erstellung von Gehäusezeichnungen von
SMD-Halbleitergehäusen -
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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

Foreword

The text of document 47D/772/FDIS, future edition 1 of IEC 60191-6-21, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-21 on 2010-10-01.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2011-07-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2013-10-01

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-21:2010 was approved by CENELEC as a European Standard without any modification. (standards.iteh.ai)

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Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60191-4	-	Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4	-
IEC 60191-6	-	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages	EN 60191-6	-

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Part 6-21: General rules for the preparation of outline drawings of surface
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dimensions of small outline packages (SOP)**

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –**Part 6-21: General rules for the preparation of outline drawings
of surface mounted semiconductor device packages –
Measuring methods for package dimensions
of small outline packages (SOP)**

FOREWORD

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International Standard IEC 60191-6-21 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/772/FDIS	47D/776/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-21: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Measuring methods for package dimensions of small outline packages (SOP)

1 Scope

This part of IEC 60191 specifies methods to measure package dimensions of small outline packages (SOP), package outline form E in accordance to IEC 60191-4.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-4, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*

[SIST EN 60191-6-21:2010](https://standards.iteh.ai/catalog/standards/sist/f91caaf1-e90f-4449-b664-948130ea001f/sist-en-60191-6-21-2010)

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3 Terms and definitions

For the purposes of this document the terms and definitions given in IEC 60191-6 apply.

4 Measuring methods

4.1 Description of measuring method

The measuring methods described in this standard are for dimension values guaranteed to users on the basis of the following items.

- a) In general, measuring the dimensions shall be made with the semiconductor packages mounted on printed circuit-board as the guarantee is made to the user.
- b) In general, measurement may be made either by hand or automatically.
- c) The dimensions that cannot be measured unless the package is destroyed may be calculated from other dimensions or replaced by representative values. See 4.6.2.3.

4.2 Reference characters and drawing

Thin small outline package TSOP (1)

An outline drawing is given in Figure 1.

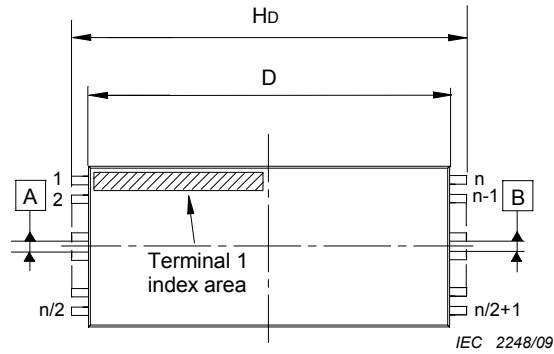


Figure 1a - Top view

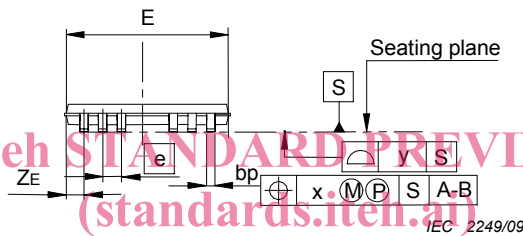


Figure 1b - Side view

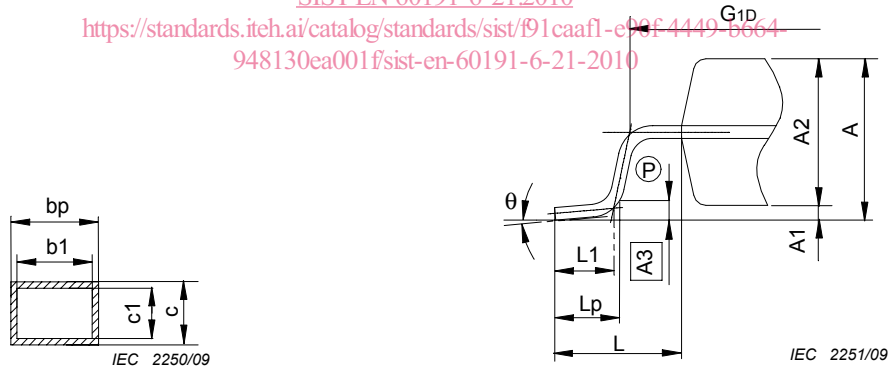


Figure 1c - Lead section

Figure 1d - Lead side view

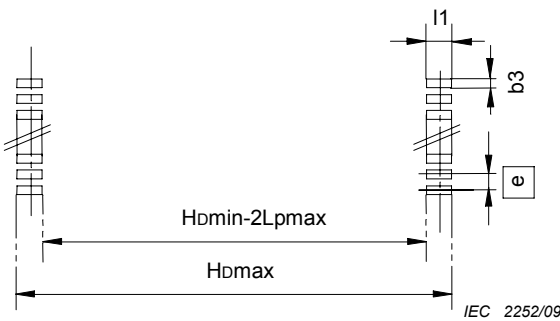


Figure 1e - Pattern of terminal position areas

Figure 1 - TSOP(1) outline drawings