IEC 60749-41

Edition 1.0 2020-07

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 41: Standard reliability testing methods of non-volatile memory devices

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 41: Méthodes d'essai normalisées pour la fiabilité des dispositifs à mémoire non volatile

IEC 60749-41:2020-07(en-fr)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

About the IEC
The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications
The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

IEC publications search - webstore.iec.ch/advsearchform
The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished
Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and once a month by email.

IEC Customer Service Centre - webstore.iec.ch/csc
If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: sales@iec.ch.

Electropedia - www.electropedia.org
The world's leading online dictionary on electrotechnology, containing more than 22 000 terminological entries in English and French, with equivalent terms in 16 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary
67 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

A propos de l'IEC
La Commission Electrotechnique Internationale (IEC) est la première organisation mondiale qui élabore et publie des Normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications IEC
Le contenu technique des publications IEC est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

Recherche de publications IEC - webstore.iec.ch/advsearchform
La recherche avancée permet de trouver des publications IEC en utilisant différents critères (numéro de référence, texte, comité d'études,…). Elle donne aussi des informations sur les projets et les publications remplacées ou retirées.

IEC Just Published - webstore.iec.ch/justpublished
Restez informé sur les nouvelles publications IEC. Just Published détaille les nouvelles publications parues. Disponible en ligne et une fois par mois par email.

Service Clients - webstore.iec.ch/csc
Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions contactez-nous: sales@iec.ch.

Electropedia - www.electropedia.org
Le premier dictionnaire d'électrotechnologie en ligne au monde, avec plus de 22 000 articles terminologiques en anglais et en français, ainsi que les termes équivalents dans 16 langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International (IEV) en ligne.

Glossaire IEC - std.iec.ch/glossary
67 000 entrées terminologiques électrotechniques, en anglais et en français, extraites des articles Termes et Définitions des publications IEC parues depuis 2002. Plus certaines entrées antérieures extraites des publications des CE 37, 77, 86 et CISPR de l'IEC.

IEC 60749-41

Edition 1.0 2020-07

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 41: Standard reliability testing methods of non-volatile memory devices

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 41: Méthodes d'essai normalisées pour la fiabilité des dispositifs à mémoire non volatile

INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

ICS 31.080.01

ISBN 978-2-8322-8640-1

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.

3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.

4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60749-41 has been prepared by IEC technical committee 47: Semiconductor devices. This standard is based on JEDEC Standard 22-A117. It is used with permission of the copyright holder, JEDEC Solid State Technology Association.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2631/FDIS	47/2643/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The stress tests described in this part of IEC 60749 are intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention).

The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. The data retention stress can be used as a proxy to replace the high temperature storage life test when the temperature and time meet or exceed qualification requirements. Cross-temperature testing for writing and reading across the data sheet temperature range can be considered when there are demonstrated sensitivities for programming at low and reading at high temperatures or vice versa. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) can be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

1 Scope

This part of IEC 60749 specifies the procedural requirements for performing valid endurance, retention and cross-temperature tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or are developed using knowledge-based methods such as in JESD94.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-6, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-23, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
cross-temperature test
CTT
data read verification across the opposite end of the operating temperature range such that when programming occurs at low temperature it is properly read at hot temperature or vice versa

Note 1 to entry: This note applies to the French language only.

3.2
cross-temperature test failure
CTTF
data read verification failure across the opposite end of the operating temperature range where it was programmed

Note 1 to entry: This note applies to the French language only.

3.3
electrically erasable programmable read-only memory
EEPROM
reprogrammable read-only memory in which the cells at each address can be erased electrically and reprogrammed electrically

Note 1 to entry: The term EEPROM in this document includes all such memories, including flash EEPROM integrated circuits and embedded memory in integrated circuits such as Erasable Programmable Logic Devices (EPLDs) and microcontrollers. Destructive-read memories such as ferroelectric memories, in which the read operation re-writes the data in the memory cells, are beyond the scope of this document.

Note 2 to entry: This note applies to the French language only.

3.4
data pattern
mix of several 1s and 0s in the memory and their physical or logical positions

Note 1 to entry: A device can be single-bit-per-cell (SBC), meaning that one physical memory cell stores a "0" or a "1", or multiple-bits-per-cell (MBC), meaning that one cell stores typically two bits of data: "00", "01", "10", or "11". In some MBC memories, the two bits represent logically-adjacent bit-pairs in each byte of data. For example, for 2 bits per cell, a byte containing binary data 10110001 would correspond to four physical cells with data 2301 in base-four logic. In other MBC memories, the two bits can represent bits in entirely different address locations. For an SBC memory a physical checkerboard pattern consists of alternating 0s and 1s, with each 0 surrounded by 1s on either side and above and below; a logical checkerboard pattern consists of data bytes AAH or 55H in which each 0 is logically adjacent to 1s. In some qualifications only logical positions are known.

3.5
endurance
ability of a reprogrammable read-only memory to withstand data rewrites and still comply with applicable specifications

Note 1 to entry: EEPROM device specifications often require an erase step before reprogramming data; in this case a data rewrite includes both erase and programming steps, which together are called a program/erase cycle. Direct-write memories allow data to be written directly over old, without an erase; in this case the use of the generic term "program/erase cycle" will refer to a single rewrite with no erase. For single-bit-per-cell (SBC) memories that require an erase step, one program/erase cycle consists of programming cells (typically to "0") and then erasing ("1"). For the comparable multiple-bits-per-cell (MBC) case, a cycle would consist of programming cells (to "0", "1", or "2" for two bits per cell) and then erasing ("3" for two bits per cell).

Note 2 to entry: Endurance cycling consists of performing multiple rewrites in succession, and the data pattern or patterns for these rewrites must be chosen. There is no one data pattern or set of patterns that is worst-case for all failure mechanisms. For example, for floating-gate memories a fully programmed pattern is worst-case for charge transfer, but a physical checkerboard pattern is worst-case for spurious programming of adjacent cells, and a mostly erased pattern can be worst-case for mechanisms related to erase-preconditioning algorithms. For MBC memories, programming to the highest state is worst-case for charge transfer, but intermediate-state cells can experience more programming time and also have less sensing margin. Finally, in some memories, the margin of a cell is influenced by the data states of the physically adjacent cells.

3.6
endurance failure
failure caused by endurance cycling

Note 1 to entry: An endurance failure occurs if, as a result of program/erase cycling, an EEPROM fails to complete the program or erase operations within the datasheet-specified times or if it fails to meet any of its other datasheet requirements. A program operation that results in incorrect data being stored in the device counts as an endurance failure. However, if an error-management method such as an error-correction code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

Note 2 to entry: Certain EEPROMS are specified to operate with either internal or external bad-block management system (BBM). When the BBM system detects an endurance failure it directs the data to another (spare) block and removes the address of the failing block from an appropriate address table. An endurance failure of such product is taken to occur when a pre-set number of spare blocks of the product had been consumed within that product datasheet specified cycle count.

Note 3 to entry: A number of distinct failure mechanisms are responsible for endurance failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters such as cycling delay between cycles. For example, in floating-gate memories, failure may be caused by charge trapping (normally accelerated by lower temperatures and/or shorter cycling delay) in the charge transfer dielectric or by oxide rupturing (normally accelerated by higher temperatures) in the transfer dielectric or in peripheral dielectrics.

3.7
failure
loss of the ability of a component to meet the electrical or physical performance specifications that (by design or testing) it was intended to meet

Note 1 to entry: The term "failure" is often qualified by an adjective describing the type of failure. For example, a component is a functional failure if it fails to function and a parametric failure if it functions but does not meet a datasheet specification for a parameter such as power consumption. Endurance and retention failures are defined in 3.6 and 3.9.

Note 2 to entry: Failures can be firm or transient. For the purpose of this standard, a firm failure is a component that fails sometime during a reliability stress and continues to fail at the final test at the end of that same stress. A transient failure is a component that fails during a reliability stress but passes in the final test at the end of that stress.

3.8
data retention
retention
ability of EEPROM cell to retain data over time

Note 1 to entry: The one-word term "retention" is usually used when context ensures that no confusion is likely; otherwise, the full term "data retention" is used.

Note 2 to entry: The term data retention can refer to the ability of a device to retain data in the unbiased state, but the term will sometimes be used to include the ability to retain data under bias. The term "disturb" refers unambiguously to the ability of an EEPROM cell to retain data over time under bias. For example, read disturb refers to the ability of an EEPROM cell to retain data after being read a given number of times. A detailed discussion of disturbs is beyond the scope of this document.

Note 3 to entry: Retention stressing consists of writing a data pattern into a device and then verifying that the pattern is intact after a specified time at a specified temperature. There is no single data pattern that is worst-case for all retention mechanisms, cell designs, or process architectures. There are generally some failure mechanisms which primarily affect programmed cells and some which primarily affect erased cells, and there are also failure mechanisms which depend on the data in adjacent cells.

3.9
data retention failure
retention failure
change of stored data by one bit or more detected when the device is read according to applicable specifications after an extended period of time following the previous write

Note 1 to entry: The short-term "retention failure" is usually used when context ensures that no confusion is likely, otherwise the full term "data retention failure" is used.

Note 2 to entry: It is necessary to distinguish whether or not retention failure was caused by charge loss or some other mechanism. Endurance cycling with shorter cycling delay between cycles might induce apparent bit change or pseudo-bit-flip.

Note 3 to entry: If an error-management method such as an error-correction-code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

Note 4 to entry: A number of distinct failure mechanisms are responsible for retention failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories, failure can occur due to defects that allow charge to leak through the transfer dielectric or by the detrapping of charge in the transfer dielectric; the former can be weakly accelerated or even decelerated by high temperature, and the latter can be highly temperature-accelerated.

3.10
uncorrectable bit-error rate
UBER
metric for the rate of occurrence of data errors, equal to the bit error rate (BER) after applying any specified error-correction method

Note 1 to entry: The uncorrectable bit error rate is calculated from the following equation:

$$k = \frac{e}{b_r} \tag{1}$$

where k is UBER,

e is the cumulative number of data errors and

b_r is the cumulative number of bits read

For non-error-corrected devices, any data bit in error counts as a data error. For error-corrected devices, any codeword or sector (as defined in the product data sheet) returning incorrect data after applying the specified error correction scheme counts as a data error. Transient data errors, such as data errors that occur at a given program/erase cycle but not at later ones, are counted as data errors. Standard statistical confidence levels can be applied to the numerator.

The cumulative number of bits read is the sum of all bits of data read back from the device, with multiple reads of the same memory bit counting as multiple bits read. For example, if a 1-Gb device is read 10 times, then there would be 10 Gb bits read.

Note 2 to entry: Some devices can be specified to have a certain UBER value, and in this case the qualification must determine that the device meets the UBER specification. Clause 5 discusses details regarding calculation of the UBER value.

4 Apparatus

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature conditions to within ±5 °C. Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the test. Also, the test circuitry should be designed so that the existence of abnormal or failed devices will not alter the specified conditions for other units on test. Care should be taken to avoid possible damage from transient voltage spikes or other conditions that might result in electrical, thermal or mechanical overstress.

5 Procedure

5.1 Qualification specifications

Qualification specifications, including those in JESD47, commonly require that some devices undergo endurance cycling followed by retention stressing. There may also be retention requirements for uncycled devices and for the optional cross-temperature testing across the temperatures specified in the data sheet. Qualification specifications commonly call for endurance cycling to be performed at multiple temperatures within the datasheet range, and retention stress to be performed both at elevated temperatures, such as 125 °C, and room temperature. Figure 1 schematically illustrates the flow, with references to the paragraphs describing the procedure.

A supplementary test condition is given in Annex A.

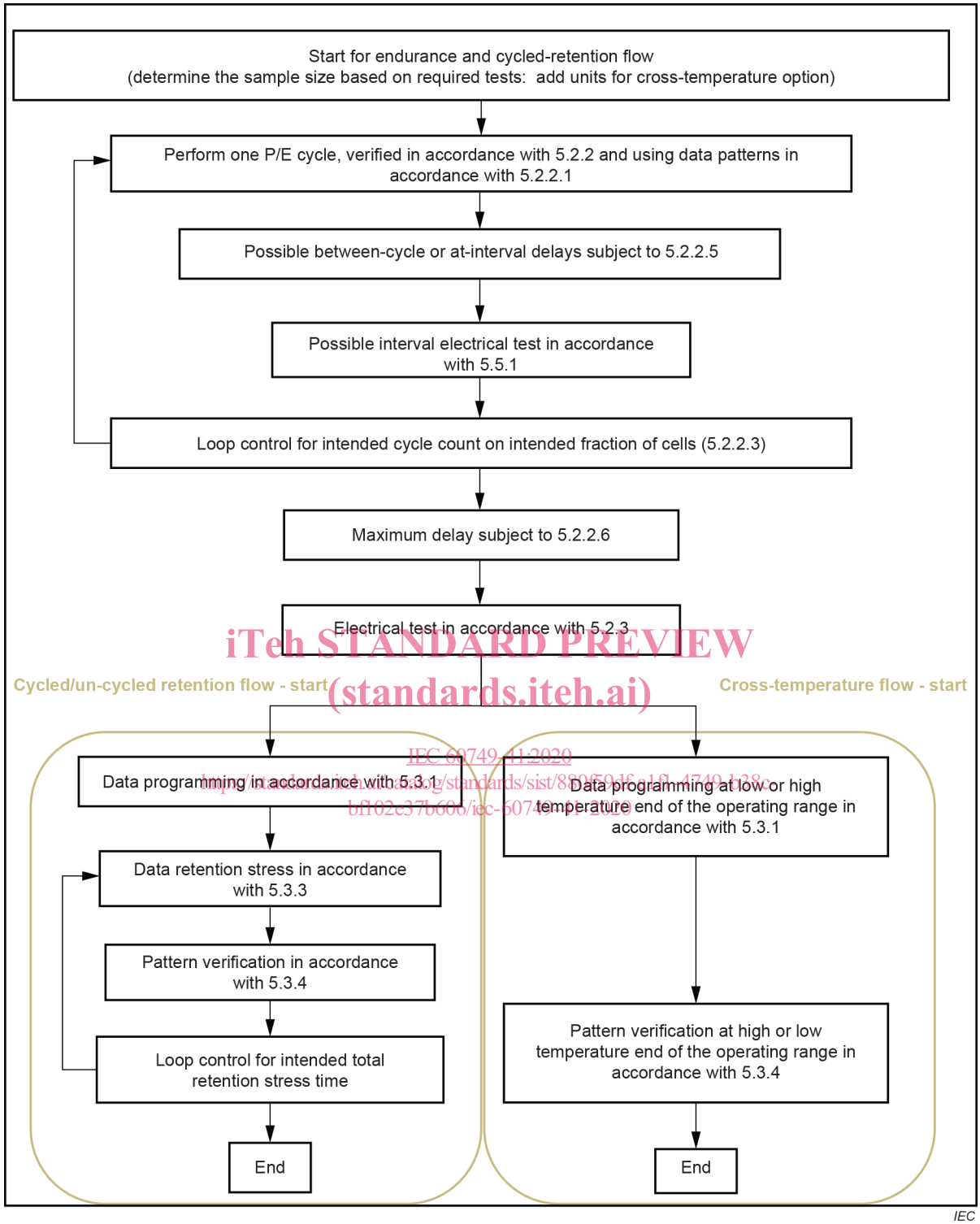

Figure 1 – Schematic flow

5.2 Program/erase endurance

5.2.1 Test setup

Devices shall be placed in the chamber so there is no substantial obstruction to the flow of air across and around each unit. The power shall be applied and suitable checks made to assure that all devices are properly energized. When special mounting or heat sinking is required, the details shall be specified in the applicable device specification and/or test specification.

5.2.2 Data cycling

5.2.2.1 Program and erase verification

Program and erase operations during the endurance test shall be verified to have been properly executed in accordance with the device specification or the supplier's internal stress test specification (see Clause 7).

5.2.2.2 Data patterns during cycling

The data pattern used for endurance cycling shall be agreed upon between supplier and user, and the rationale documented. It is important to cycle enough sectors of blocks during the cycling period taking into account for the target application models. See Note 1 to Entry 3.4 for a discussion of the trade-offs involved in the selection of data pattern for cycling.

The purpose of many qualifications is to test the device for the broadest possible range of failure mechanisms. The broadest possible range of failure mechanisms can be detected when the data pattern includes the full range of logic levels and adjacency conditions that would occur in actual use. For example, this full range can be achieved if the following three conditions are met. First, the data in the memory cells is cycled between all available logic states in equal measure. For example, in an SBC memory half the cells would be programmed and half left erased in any one cycle, whereas in a 4-level cell memory one-quarter of the cells would be written to each of the four available levels in any given cycle. Second, the positions of 1s and 0s are non-uniform, ideally quasi-random, so that all possible adjacency configurations are represented. For example, a data pattern consisting of a mix of bytes with data patterns 00H (zero zero hexadecimal), 55H, AAH, 33H, CCH, and FFH would create a wide range of adjacency patterns. Third, the data pattern in successive cycles is not the same, but rather follows a sequence. Best practice is to ensure, in this sequence, that some cells are written to all available logic states while other cells are re-written to the same logic state in every cycle. For example, in an SBC memory, a byte that was cycled to AAH in even-numbered cycles and 5AH in odd-numbered cycles would have four cells that would be written to 0s and 1s in alternating cycles, two cells that are re-written to 0 in every cycle, and two cells that are re-written to 1 in every cycle.

In some knowledge-based qualifications, endurance tests can be defined for specific failure mechanisms. Such tests can use different data patterns from that described above, optimized to increase the sensitivity to the targeted mechanisms. Examples of acceptable data patterns for such purposes include a solid programmed pattern, checkerboard/inverse-checkerboard sequence, and checkerboard with subsequent filling-in of the pattern.

Some flash EEPROM devices employ a built-in scrambling mechanism. When testing endurance of such devices, the scrambling mechanism should be enabled; disabling the scrambler for endurance cycling can stress the product beyond the stress a user can experience. A quasi-random pattern is best for testing endurance when employing scrambling.

5.2.2.3 Fraction of cells to be cycled

Qualification specifications, whether from JESD47 or developed using knowledge-based methods (JESD94) will generally require that some fraction of the memory to be cycled to the maximum number of program/erase cycles specified in the device specification and other fractions to be cycled to lesser amounts. In large memories, it can take a prohibitively long time to cycle all cells to the maximum specification, and in knowledge-based qualifications it is possible that application use conditions do not require all cells to be so cycled. The actual fraction of cells cycled to 100 % of the maximum specification, and the fraction cycled to other percentages of the specification, shall be agreed upon between supplier and user and documented, along with the rationale for the chosen fractions.