SIST

SLOVENSKI STANDARD
SIST EN 60191-6-17:2011

01-junij-2011

Standardizacija mehanskih lastnosti za polprevodniške elemente - 6-17. del: Splošna pravila za pripravo tehničnih risb za polprevodniške elemente v okrovih za površinsko montažo - Navodilo za oblikovanje zloženih okrovov - Vezja s finim rastrom mreže krogličnih priključkov in finim rastrom mreže priključkov v ravnini (P-PFBGA in P-PFLGA) (IEC 60191-6-17:2011)

Mechanical standardization of semiconductor devices - Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and PPFLGA) (IEC 60191-6-17:2011)

Mechanische Normung von Halbleiterbauelementen - Teil 6-17: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für gestapelte Gehäuse - Feinraster-Ball-Grid-Array und Feinraster-Land-Grid-Array (P-PFBGA/P-PFLGA) (IEC 60191-6-17:2011)

Normalisation mécanique des dispositifs à semiconducteurs - Partie 6-17: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface - Guide de conception pour les boîtiers emplilés - Boîtiers matriciels à billes et à pas fins et boîtiers matriciels à zone de contact plate et à pas fins (P-PFBGA et P-PFLGA) (CEI 60191-6-17:2011)

Ta slovenski standard je istoveten z: EN 60191-6-17:2011

ICS:

01.100.25	Risbe s področja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

SIST EN 60191-6-17:2011 en

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60191-6-17

April 2011

ICS 31.080.01

English version

Mechanical standardization of semiconductor devices - Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

(IEC 60191-6-17:2011)

Normalisation mécanique des dispositifs à semiconducteurs -
Partie 6-17: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface -
Guide de conception pour les boîtiers emplilés -
Boîtiers matriciels à billes et à pas fins et boîtiers matriciels à zone de contact plate et à pas fins (P-PFBGA et P-PFLGA)
(CEI 60191-6-17:2011)

Mechanische Normung von Halbleiterbauelementen -
Teil 6-17: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen -
Konstruktionsleitfaden für gestapelte Gehäuse -
Feinraster-Ball-Grid-Array und Feinraster-Land-Grid-Array (P-PFBGA/P-PFLGA)
(IEC 60191-6-17:2011)

This European Standard was approved by CENELEC on 2011-03-03. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

Foreword

The text of document 47D/785/FDIS, future edition 1 of IEC 60191-6-17, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-17 on 2011-03-03.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2011-12-03
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2014-03-03

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-17:2011 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-6	-	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages	EN 60191-6	-
IEC 60191-6-5	-	Mechanical standardization of semiconductor devices - Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)	EN 60191-6-5	-

IEC 60191-6-17

Edition 1.0 2011-01

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices –
Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

Normalisation mécanique des dispositifs à semiconducteurs –
Partie 6-17: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface – Guide de conception pour les boîtiers empilés – Boîtiers matriciels à billes et à pas fins et boîtiers matriciels à zone de contact plate et à pas fins (P-PFBGA et P-PFLGA)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX U

ICS 31.080.01

ISBN 978-2-88912-331-5

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-17 has been prepared by subcommittee 47D: Mechanical standardization for semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/785/FDIS	47D/793/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

The trend toward downsizing and higher density of portable electronic devices has driven LSI packages into smaller and higher density configurations. The market demand of higher density has led to the development of the package stacking technology that enabled miniaturization and higher functionality. The objective of this design guide is to standardize outlines and to get interchangeability of individual stackable packages.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

1 Scope

This part of IEC 60191 provides outline drawings and dimensions for stacked packages and individual stackable packages in the form of FBGA or FLGA.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document applies.

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device package*

IEC 60191-6-5, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60191-6 and the following apply.

3.1
individual stackable package
package with an array of metallic balls or lands on the underside of the package for the purpose of surface-mount on a printed circuit board and an array of footprints (lands) on the upper side of the package for stacking packages

NOTE The individual stackable cavity-up FLGA package is a part of this specification on the premise of stacking a cavity-down FBGA with cavity-up FLGA.

3.2
stacked package
assembly of multiple individual stackable packages in a stacked configuration

NOTE The top package can be a standard FBGA specified in IEC 60191-6-5 without any footprints on the upper side of the package. The stand-off height of this standard package, however, shall follow this design guide.

3.3
mould cap height (A_2)
height of the mould cap which contains wire-bonded die or of the exposed flip chip-bonded die with respect to the upper substrate surface of the package