SLOVENSKI STANDARD
SIST EN 60749-29:2011

01-oktober-2011

Polprevodniški elementi - Mehanske in klimatske preskusne metode - 29. del: Preskus zapore

Semiconductor devices - Mechanical and climatic test methods - Part 29: Latch-up test

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 29: Essai de verrouillage

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Ta slovenski standard je istoveten z: EN 60749-29:2011

ICS:

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

SIST EN 60749-29:2011 en

2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

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EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60749-29

August 2011

ICS 31.080.01

Supersedes EN 60749-29:2003 + corr. Mar.2004

English version

Semiconductor devices -
Mechanical and climatic test methods -
Part 29: Latch-up test
(IEC 60749-29:2011)

Dispositifs à semiconducteurs -
Méthodes d'essai mécaniques et climatiques -
Partie 29: Essai de verrouillage
(CEI 60749-29:2011)

Halbleiterbauelemente -
Mechanische und klimatische Prüfverfahren -
Teil 29: Latch-up-Prüfung
(IEC 60749-29:2011)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
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Ref. No. EN 60749-29:2011 E

SIST EN 60749-29:2011

Foreword

The text of document 47/2083/FDIS, future edition 2 of IEC 60749-29, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60749-29 on 2011-05-12.

This European Standard supersedes EN 60749-29:2003 + corrigendum March 2004.

The significant changes with respect to EN 60749-29:2003 include:

– a number of minor technical changes;

– the addition of two new annexes covering the testing of special pins and temperature calculations.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2012-02-12
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2014-05-12

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Endorsement notice

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The text of the International Standard IEC 60749-29:2011 was approved by CENELEC as a European Standard without any modification.

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IEC 60749-29

Edition 2.0 2011-04

INTERNATIONAL STANDARD

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Part 29: Latch-up test**

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INTERNATIONAL
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INTERNATIONALE

PRICE CODE
CODE PRIX T

ICS 31.080.01

ISBN 978-2-88912-434-3

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SIST EN 60749-29:2011

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

FOREWORD

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International Standard IEC 60749-29 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2003 and constitutes a technical revision. The significant changes with respect to the previous edition include:

– a number of minor technical changes;
– the addition of two new annexes covering the testing of special pins and temperature calculations.

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2083/FDIS	47/2090/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

1 Scope and object

This part of IEC 60749 covers the I-test and the overvoltage latch-up testing of integrated circuits.

This test is classified as destructive.

The purpose of this test is to establish a method for determining integrated circuit (IC) latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are used in determining product reliability and minimizing "no trouble found" (NTF) and "electrical overstress" (EOS) failures due to latch-up.

This test method is primarily applicable to CMOS devices. Applicability to other technologies must be established.

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The classification of latch-up as a function of temperature is defined in 3.1 and the failure level criteria are defined in 3.2

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2 Terms and definitions

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For the purposes of this document, the following terms and definitions apply.

2.1
cool-down time
period of time between successive applications of trigger pulses or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse (See Figures 4, 5, and 8 and Table 2.)

2.2
device under test
DUT
semiconductor product subjected to latch-up test

2.3
ground
GND
common or zero-potential pin(s) of the DUT

NOTE 1 Ground pins are not latch-up tested.

NOTE 2 A ground pin is sometimes called V_{ss}.

2.4
input pins
all address, data-in control, V_{ref} and similar pins

2.5
I/O (bi-directional) pins
device pins that can be made to operate as an input or output or in a high-impedance state

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2.6
I_{supply}
total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in Table 1

2.7
I-test
latch-up test that supplies positive and negative current pulses to the pin under test

2.8
latch-up
state in which a low-impedance path resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

2.9
logic-high
level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, a voltage level equal to V_{supply} is used for latch-up testing, except where otherwise specified in the relevant specification.

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NOTE 2 For non-digital devices, V_{supply} voltage level or the maximum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

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2.10
logic-low
level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, ground voltage level is used for latch-up testing, except where specified in the relevant specification.

NOTE 2 For non-digital devices, ground voltage level or the minimum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

2.11
maximum V_{supply}
maximum operating voltage for operation within performance specifications

NOTE 1 The maximum voltage is not the absolute maximum voltage beyond which permanent damage is likely.

NOTE 2 Maximum refers to the magnitude of V_{supply} and can be either positive or negative.

2.12
no connect pin
pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device

NOTE All “no connect” pins should be left in an open (floating) state during latch-up testing.

2.13
nominal I_{supply} (I_{nom})
measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in Clause 5 and Table 1

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2.14
output pin
device pin that generates a signal or voltage level as a normal function during the normal operation of the device

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

2.15
preconditioned pin
device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT

2.16
testing of dynamic devices
latch-up trigger testing of a device in a known stable state, at the minimum-rated clock frequency applied to the device (see 5.2.3 for specified conditions)

2.17
test condition
test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test

2.18
timing-related input pin
pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a normal operating mode

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NOTE Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

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2.19
trigger pulse
positive or negative current pulse (I-Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up (see Figures 4, 5 and 8)

2.20
trigger duration
duration of an applied pulse from the trigger source (see Figures 4, 5 and 8 and Table 2)

2.21
V_{supply} pin (or pin group)
all DUT power supply and external voltage source pins (excluding ground pins), including both positive- and negative-potential pins

NOTE 1 Generally, it is permissible to treat equal potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When forming V_{supply} pins (or pin groups), the combination of V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

2.22
V_{supply} overvoltage test
latch-up test that supplies overvoltage pulses or overvoltage d.c. level to the V_{supply} pin under test

2.23
V_{supply} voltage level
applicable voltage level of the V_{supply} pin specified in the relevant specification. The V_{supply} voltage level is used for latch-up testing as the typical logic high level unless otherwise specified (see 2.9)