IEC PAS 62878-2-5

Edition 1.0 2015-08

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

colour inside

Device embedded substrate – Guidelines – Data format

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FOREWORD

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IEC PAS 62878-2-5 was submitted by the JPCA (Japan Electronics Packaging and Circuits Association) and has been processed by IEC technical committee 91: Electronics assembly technology.

It is based on JPCA-EB02 (2011). It is published as a double-logo IEC / JPCA PAS.

The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document
Draft PAS	**Report on voting**
91/1257/PAS	91/1264/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

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DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

1 Scope

This part of IEC 62878 defines the data format for active and passive devices embedded inside an organic board whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material. The basic structures, the terminology, reliability tests and a design guide are described in the “Standard of device embedded substrate", JPCA EB01, fourth edition.

A device embedded substrate contains device(s) in the board and is connected in a 3D way. Conventional 2D design technology using GERBER format cannot describe all the connection information in a device embedded substrate. We have several proposals to express 3D data formats but they cannot describe the structures given in EB01. The JPCA Committee for standardization of device embedded substrates has studied various formats and developed a format, FUJIKO V-1.0, which can express substrate design data in CAM data used in actual production. This Publicly Available Specification (PAS) described the FUJIKO data format.

Figure 1.1 shows the design flow of a device embedded substrate. The design data can be directly sent to a board manufacturing system using the FUJIKO format, or can be converted to CAM data and then be used in production. The data contain 3D information of coordinates and shapes of devices used. It is possible to check the status of device embedding in a board, and also make it a common knowledge in production know-how of a production line.

This PAS describes the expression of 3D data information, the concept of layers, the structure of board data, and definitions of information repeatedly used in design.

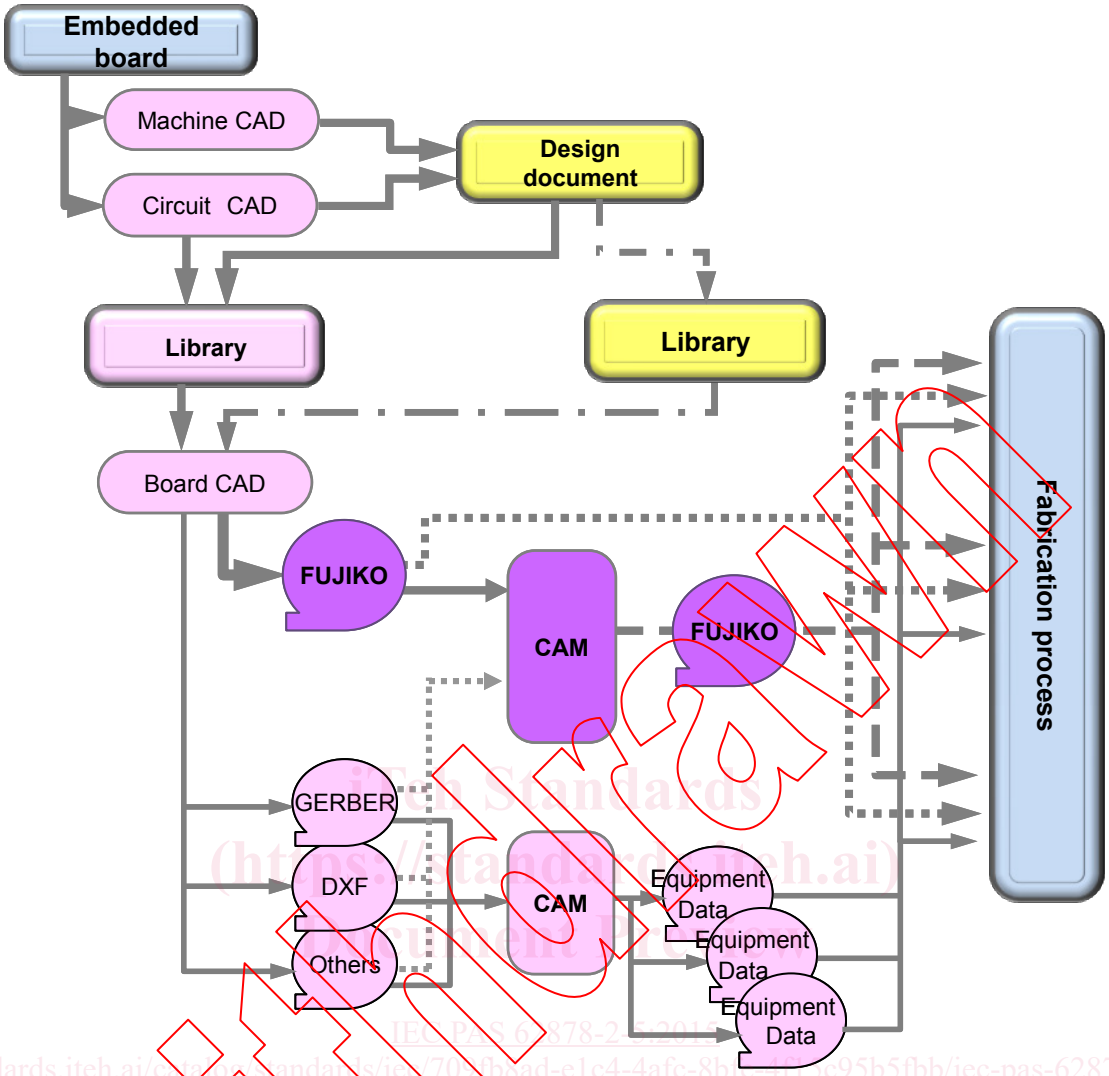


Figure 1.1 – Flow chart of design of device embedded substrate

1.1 Purpose

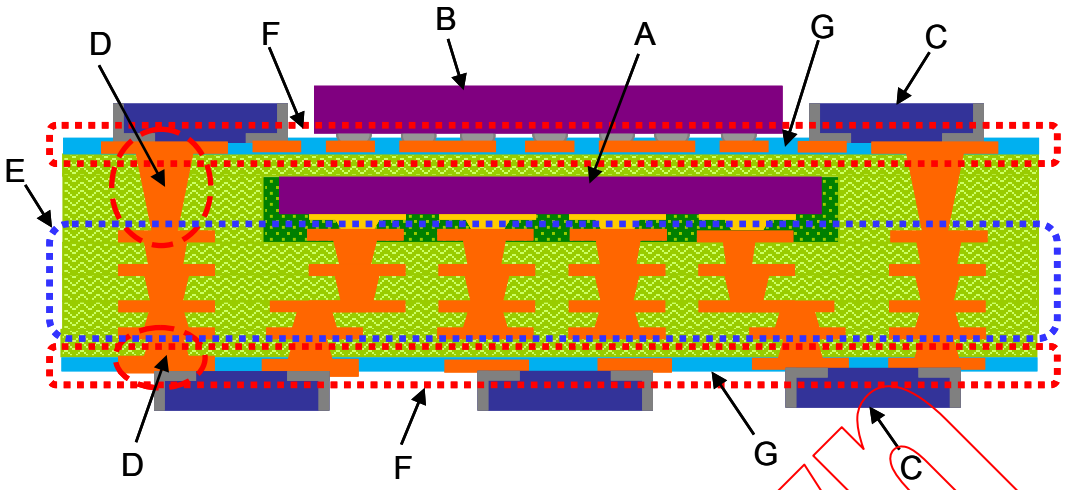
This file format describes the detailed 3D information of the following electronic circuit boards including device embedded substrate and SiP (system in package), and makes it possible to use necessary information from the stage of design to fabrication of products.

1.2 Applicable range

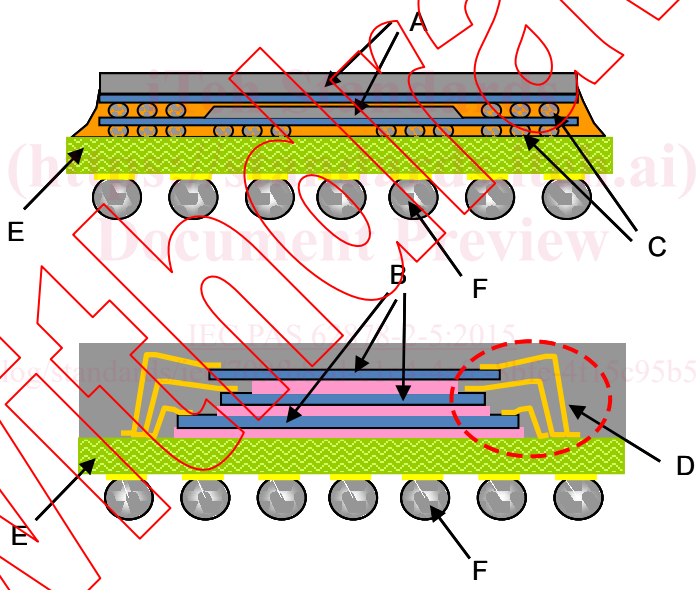
1.2.1 Product

It is possible to maintain the following design information of device embedded substrate as shown in Figure 1.2.

1) Information of inside device embedded substrate and surface mounting.
2) Assembly information of SiP (System in Package).



A	Embedded active device	E	Inner pattern
B	Surface mounted active device	F	Surface pattern
C	Surface mounted passive device	G	Solder resist
D	Layer connecting via		



A	CSP	D	Wire bonding
B	Bare die semiconductor device	E	Interposer
C	Solder ball	F	Solder ball

Figure 1.2 – General concept of product

1.2.2 Process

The format describes maintained and available information of each stage in production as described in Figure 1.1

1) Design
2) Simulation
3) Substrate fabrication
4) Device embedding
5) Test.

Table 1.1 – Information required in production

Process	Holding data of	Data available for
Design	Circuit Components Shape of the board Board structure Design/Production rule (for check)	Limited condition Net list
Simulation	Circuit Characteristics of components Board properties (materials) Board structure Art work	Electrical properties Thermal properties Mechanical properties Electronic properties Additional information in production
Substrate fabrication	Art work Drilling Symbol marks Panel format	Equipment Additional information in production
Device embedding	Component shape Embedding position Interconnection terminals Symbol marks	Equipment Relative positions of component Component list
Test	Art work Component shape Component position Terminal information Marks	Electrical test equipment Video image inspection

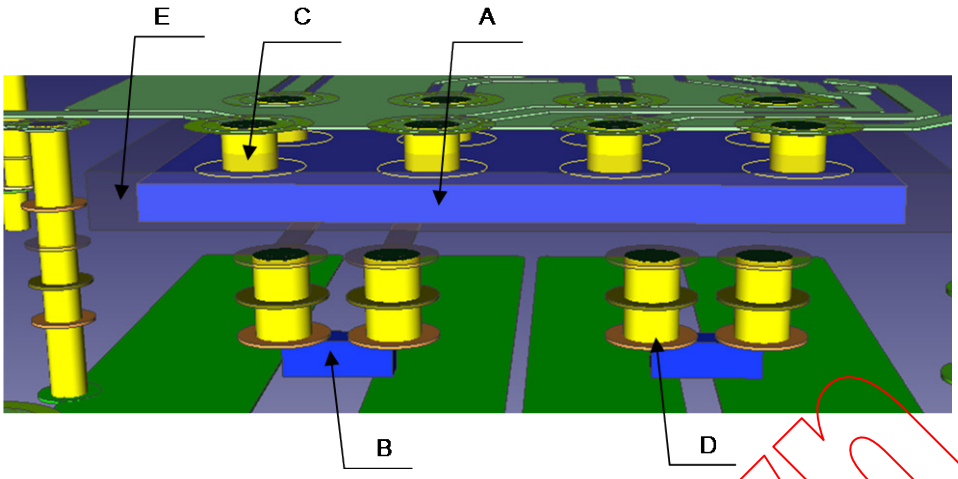
1.3 Features

Data format has the following characteristics:

1) can contain the structure of the device embedding substrate specified inEB01;
2) can contain information of SiP in general (chip stack, PoP TSV, wire bonding, flip-chip, interposer, etc.);
3) design data of terminal positions of embedding device in a virtual layer specified in EB01;
4) information of internal structure of devices such as SiP which cannot be described as a structure of a device embedded substrate and of a terminal structure as 3D design data;
5) seamless keeping of design data of devices having different level such as SiP and of embedding substrate.

1.3.1 Maintenance of the device embedded substrate structure

It is possible to keep and illustrate the 3D structure of device embedded substrate as shown in Figure 1.3. It is also possible to check its 3D structure.

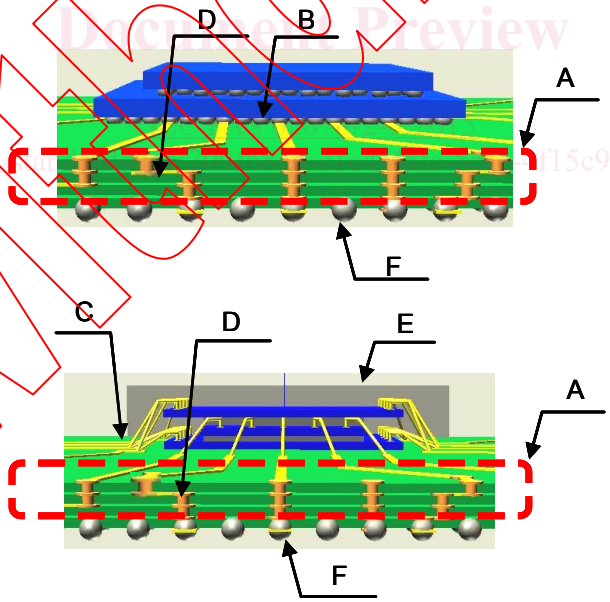


A	Embedded active device	D	Pad connection
B	Embedded passive device	E	Space without board material
C	Via connection		

Figure 1.3 – Example of a structure of a device embedded substrate

1.3.2 Maintenance of SiP interposer structure

It is possible to keep and illustrate the 3D structure of SiP substrate as shown in Figure 1.4. It is also possible to check structures of flip-chip and wire bonding mounting.



A	Interposer	D	Interposer
B	Flip-chip connection	E	Package
C	Wire bonding connection	F	Solder ball

Figure 1.4 – Examples of a structure of a SiP interposer

1.3.3 Maintenance of design data with a virtual layer of terminal positions of embedded device(s)

It is possible to keep the design data defined in EB01 of the terminal position of a via connection not on a conductor layer, but as in a virtual layer. It can be maintained in the structure shown in Figure 1.5.