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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Integrated circuits – EMC evaluation of transceivers –
Part 1: General conditions and definitions

Circuits intégrés – Évaluation de la CEM des émetteurs-récepteurs –
Partie 1: Conditions générales et définitions

IEC 62228-1:2018-01(en-fr)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTEGRATED CIRCUITS – EMC evaluation of transceivers –

Part 1: General conditions and definitions

FOREWORD

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International Standard IEC 62228-1 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

This bilingual version (2019-02) corresponds to the monolingual English version, published in 2018-01.

The text of this International Standard is based on the following documents:

CDV	Report on voting
47A/1018/CDV	47A/1034/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The French version of this document has not been voted upon.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62228 series, published under the general title *Integrated circuits – EMC evaluation of transceivers*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTEGRATED CIRCUITS – EMC evaluation of transceivers –

Part 1: General conditions and definitions

1 Scope

This part of IEC 62228 provides general information and definitions for electromagnetic compatibility (EMC) evaluation of integrated circuits (IC) with transceivers for wired network applications under network condition. It defines general test conditions, general test setups and test and measurement methods are applied to all parts of IEC 62228.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 1: General conditions and definitions*

IEC 61967-4:2002, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method*
IEC 61967-4:2002/AMD1:2006

IEC 62132-1, *Integrated circuits – Measurement of electromagnetic immunity – Part 1: General conditions and definitions*

IEC 62132-4, *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*

IEC 62215-3, *Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method*

ISO 10605, *Road vehicles – Test methods for electrical disturbances from electrostatic discharge*

3 Terms, definitions and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 61967-1 and IEC 62132-1 as well as the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1 Terms and definitions

3.1.1
global pin
carries a signal or power that enters or leaves the application board without any active component in between

3.1.2
mandatory components
components needed for proper function of the IC as specified by the IC manufacturer (e.g. application note)

3.2 Abbreviated terms

DUT device under test
DPI direct RF power injection
ESD electrostatic discharge
PCB printed circuit board
RxD receive data
SBC system base chip
TxD transmit data

4 Philosophy

The intention of this document is to provide general definitions to evaluate the EMC performance of transceiver ICs under application-like conditions in a minimal network by applying standardized IC EMC test methods. The goal is to define guidelines for the EMC characterisation on dedicated global pins of transceiver ICs that are considered EMC-relevant in the application.

The evaluation of the EMC characteristics of transceivers shall be performed in functional operation modes under minimal network conditions with two transceivers for RF emission, RF immunity and impulse immunity tests. For electrostatic discharge tests related to packaging and handling of assembled devices, a single unpowered transceiver IC shall be evaluated.

The test methods used for the EMC characterization are based on the international standards for IC EMC tests and are described in Table 1.

Table 1 – Overview of test and measurement methods

Transceiver mode	Required test	Test method
Functional (powered)	RF emission	150 Ω direct coupling (IEC 61967-4)
	RF immunity	DPI (IEC 62132-4)
	Impulse immunity	Non-synchronous transient injection (IEC 62215-3)
Passive (unpowered)	ESD	Contact discharge (ISO 10605)

The 150 Ω direct coupling, DPI and non-synchronous transient injection test methods are chosen for the evaluation of the EMC characteristics of transceivers in functional modes.

These three test methods are based on the same approach using conductive coupling. Therefore, it is possible to use the same test board for all tests in functional operation mode, which increases the reproducibility and comparability of test results.

The test configuration in general consists of two transceivers with mandatory external components and components for filtering (e.g. bus filter) and decoupling in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling ports are connected as shown in Figure 1.

In specific cases or for analyses, a deviation from this setup can be agreed upon between the users of this document and will be noted in the test report.

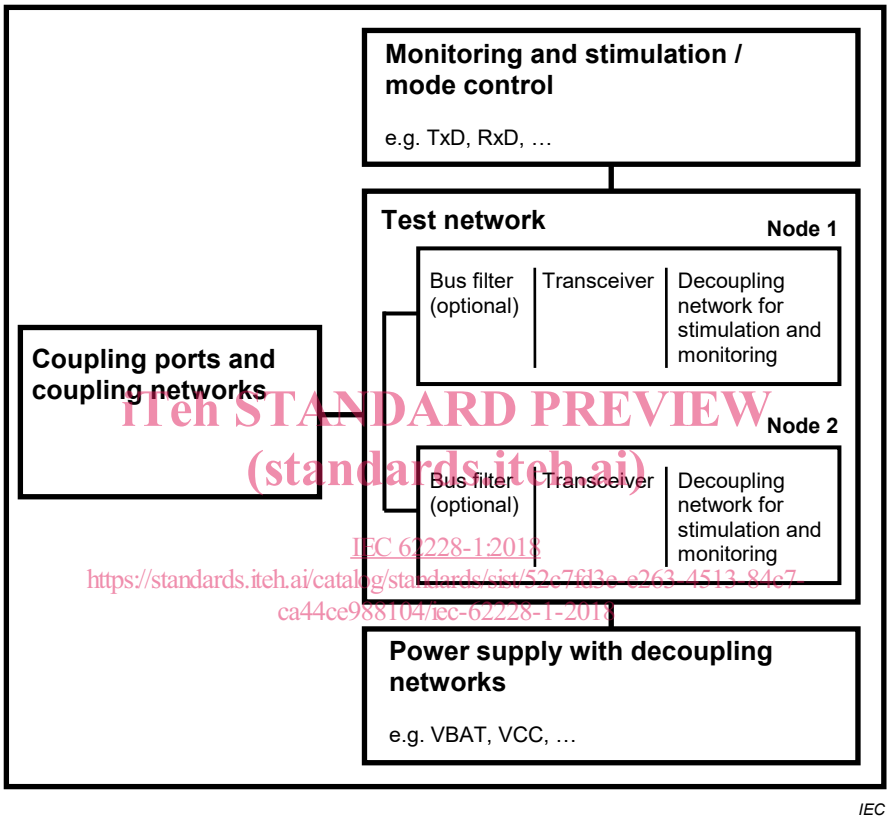

Figure 1 – General test configuration for tests in functional operation modes

The general test configuration for the unpowered ESD test of transceiver ICs consists of a single transceiver IC with mandatory external components and components for filtering on a test board with discharge coupling ports as shown in Figure 2.

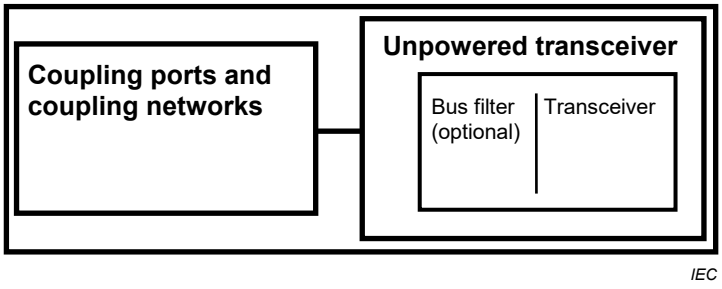

Figure 2 – General test configuration for unpowered ESD test

5 General test conditions and test board specification

5.1 Test conditions

For the purposes of this document, the test conditions given in IEC 61967-1, IEC 62132-1, IEC 62215-3 and ISO 10605 apply for the related test methods.

These test conditions are intended to ensure a consistent test environment. If the users of this procedure agree to use other values, they shall be documented in the test report.

5.2 Test board specification

For functional tests of transceiver ICs, the test network shall be designed on a printed circuit board. To ensure good RF characteristics of the coupling and decoupling, an equal design of the circuitry for node 1 and 2 on a minimum two-layer PCB with a GND layer should be used. The length of the coupling paths on the test board should be kept as short as possible. The trace length for bus interconnections should be shorter than 30 mm from the star point of the interconnection to the IC pins when applicable. The test PCB's injection ports shall be designed free of resonances in the target frequency range. The DUT shall be soldered on the test board to minimize parasitic effects. For proper shielding, all connections to the test peripheral of the test board should be realized through coaxial printed circuit board sockets except for the filtered power supplies and GND.

For ESD tests, a printed circuit board shall be used. At a minimum, a two-layer construction of the PCB with GND layer shall be chosen. The pads for the discharge points shall be carried out in a way that a proper contact to the discharge tip of the test generator is ensured (e.g. by rounded vias in the layout of the ESD test board). The discharge point shall be directly connected by a trace to the respective pin under test of the transceiver IC. The passive components of the network shall be placed close to the transceiver IC to reduce parasitic effects. The DUT should be soldered on the test board to ensure application-like conditions and avoid parasitic setup effects by sockets. The insulation distance between the signal lines and pads of the passive components and the extensive ground area should be designed in a way that a spark over at these points can be prevented up to the intended test voltage level.

Dedicated layout examples are provided within the respective parts of this series of standards.

Further layout recommendations are given in IEC 62132-1, IEC 62132-4, IEC 61967-1 and IEC 61967-4.

6 Test report

For the purposes of this document, the test report definitions given in IEC 61967-1, IEC 62132-1, IEC 62215-3 and ISO 10605 apply for the respective test methods.

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