

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Device embedding assembly technology –
Part 1: Generic specification for device embedded substrates
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Techniques d'assemblage avec appareils intégrés –
Partie 1: Spécification générique pour substrats avec appareils intégrés

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**Device embedding assembly technology –
Part 1: Generic specification for device embedded substrates**

**Techniques d'assemblage avec appareils intégrés –
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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 1: Generic specification for device embedded substrates

FOREWORD

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International Standard IEC 62878-1 has been prepared by IEC technical committee 91: Electronics assembly technology.

This bilingual version (2020-03) corresponds to the monolingual English version, published in 2019-10.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
91/1597/FDIS	91/1616/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
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INTRODUCTION

This document is a generic specification for device-embedded substrates fabricated by embedding discrete active and/or passive electronic devices into one or multiple inner layers of an organic substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Other special technologies for the realization of conductive or isolating structures and electronic components functions inside of substrates, like electronic modules or redistribution layers of integrated circuit packages are not covered by this document.

The device-embedded substrate can be used as a substrate to mount SMDs or THDs to form electronic circuits, as conductor and insulator layers can be formed after embedding electronic devices.

The purpose of this series of documents is to obtain common understanding in structures, test methods, design and fabrication processes and use of device-embedded substrate in the industry. These documents do not specify details of the manufacturing processes, design criteria and requirements, as those normally constitute intellectual property of the manufacturers and are very specific to the individual embedding technologies and applications.

Generic specification

The generic specification covers all subjects mainly common to device-embedded substrates for use in electronic equipment, such as terminology, methods of measurement and tests. Where the individual subjects require the prescription of conditions or parameters specific to the particular sub-family or type of embedded substrates, such prescriptions are required to be given by one of the subordinate specifications.

[IEC 62878-1:2019](https://standards.iteh.ai/catalog/standards/sist/0e817376-1e1d-47d7-8500-0cb13cda5db3/iec-62878-1-2019)

The numeric reference of the generic specification is IEC 62878-1.

Sectional and detail specifications (requirements to technology and components)

Sectional specifications cover all subjects additional to those given in the generic specification, which are specific to a defined sub-group of device-embedded substrate technologies. These subjects normally are preferred values for characteristics, additional test methods and relevant prescriptions for test methods given in the generic specification, prescriptions for sampling and for the preparation of specimens, recommended test severities and preferred acceptance criteria. The sectional specification also outlines the structure and scope of the test schedules that are to be applied in all subordinate detail specifications.

The numeric reference of the sectional and related detail specifications is IEC 62878-3-x.

Guidelines and supporting documentation

Supporting documentation and guidelines provide information in addition to the provisions of generic, sectional and detail specifications.

The numeric reference of supporting documentation and guidelines is IEC 62878-2-x.

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 1: Generic specification for device embedded substrates

1 Scope

This part of IEC 62878 specifies the generic requirements and test methods for device-embedded substrates. The basic test methods for printed board substrate materials and substrates themselves are specified in IEC 61189-3.

This part of IEC 62878 is applicable to device-embedded substrates fabricated by use of organic base material, which includes, for example, active or passive devices, discrete components formed in the fabrication process of electronic printed boards, and sheet-formed components.

The IEC 62878 series applies neither to the re-distribution layer (RDL) nor to electronic modules defined in IEC 62421.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[IEC 62878-1:2019](https://standards.iteh.ai/catalog/standards/sist/0c817276-1a1d-47d7-8500-6003da5d57cc/iec-62878-1-2019)

IEC 60068-2-1, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60068-2-2, *Environmental testing – Part 2-2: Tests – Test B: Dry heat*

IEC 60068-2-6, *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60068-2-21, *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*

IEC 60068-2-27, *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*

IEC 60068-2-69, *Environmental testing – Part 2-69: Tests – Test Te/Tc: Solderability testing of electronic components and printed boards by the wetting balance (force measurement) method*

IEC 60068-2-78, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60194-2, *Printed board design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC 61340-5-3, *Electrostatics – Part 5-3: Protection of electronic devices from electrostatic phenomena – Properties and requirements classification for packaging intended for electrostatic discharge sensitive devices*

IEC 61760-4, *Surface mounting technology – Part 4: Classification, packaging, labelling and handling of moisture sensitive devices*

IEC 62137-1-4, *Surface mounting technology – Environmental and endurance test methods for surface mount solder joint – Part 1-4: Cyclic bending test*

IEC 62878-1-1, *Device embedded substrate – Part 1-1: Generic specification – Test methods*

IEC TS 62878-2-1, *Device embedded substrate – Part 2-1: Guidelines – General description of technology*

IEC TR 62878-2-2, *Device embedded substrate – Part 2-2: Guidelines – Electrical testing*

IEC TS 62878-2-3, *Device Embedded Substrate – Part 2-3: Guidelines – Design Guide*

IEC TS 62878-2-4, *Device Embedded Substrate – Part 2-4: Guidelines – Test element groups (TEG)*

J-STD 033, *Handling, Packing, Shipping, and Use of Moisture/Reflow and/or Process Sensitive Components*

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3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

device-embedded substrate

DES

substrate in which one or more active devices (semiconductor device) and/or passive devices (e.g. resistor or capacitor) are formed using thick-film technology or by embedding them within the substrate

4 Value chain

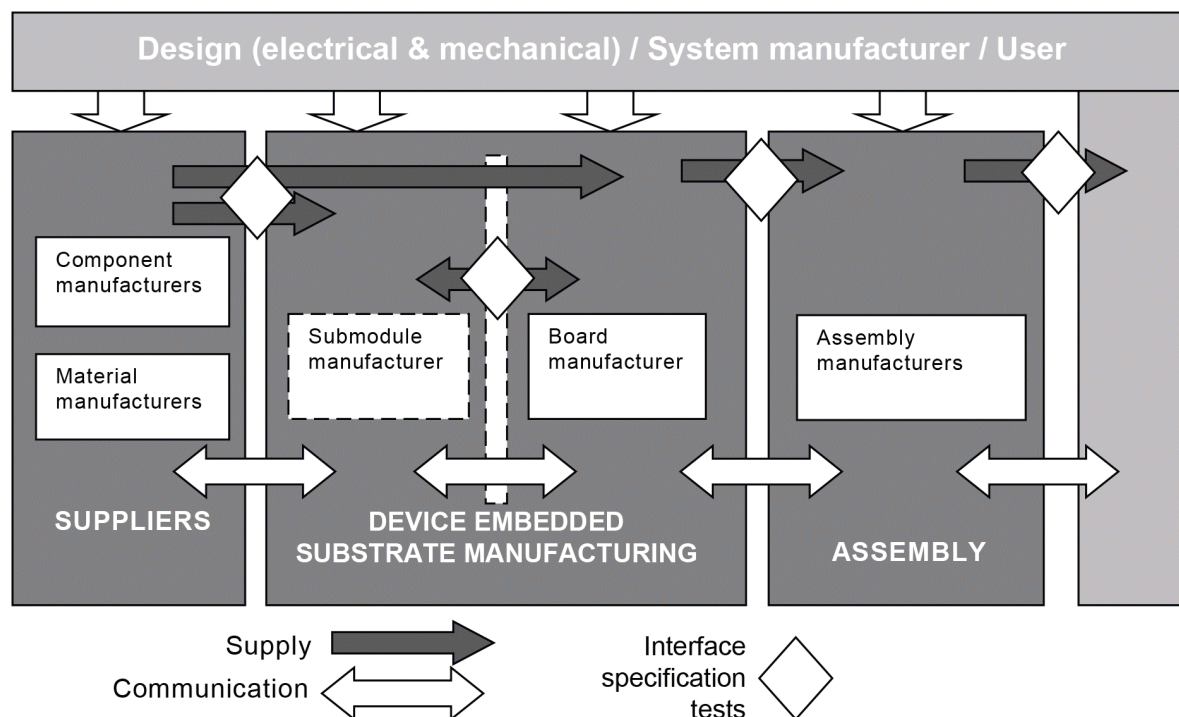
4.1 System description

4.1.1 Generic design variants

Generic design variants are described in IEC TS 62878-2-1.

4.1.2 Generic value chain

The business model shown in Figure 1 shows the supply routes and communication along the value chain.



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Figure 1 – Value chain and interfaces
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4.2 Elements of the value chain

4.2.1 General

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All materials have to be aligned with the embedding technology and the components to be embedded. Composition and processability of the materials and components for embedding shall be compatible.

The detail specification for the base material shall be defined by the board or submodule manufacturer. Generic specifications such as "FR4" are not specific enough.

4.2.2 System manufacturer

The requirements to the electronic system normally are determined by the system (equipment) manufacturer and can contain requirements such as functionality, use conditions (environmental and electrical), field performance, reliability, useful lifetime, restriction of substances and further customer-specific requirements. These requirements shall be deployed through the total value chain, e.g. by requirement sheets, so that assembly design and processing, device-embedded substrate design and processing, as well as the components and materials fit together, and can contribute to the fulfilment of those requirements. The strategy for electrical tests shall be planned and confirmed by the involved partners in accordance with IEC 62878-1-1 and IEC TR 62878-2-2, taking into consideration component test specifications and tests at board and system level.

This deployment process can be supported in form of a failure mode and effect analysis (FMEA) or by similar tools. A concept for the qualification of processes, components and materials shall be agreed at a very early stage of development (see also IEC TS 62878-2-4).

4.2.3 Components manufacturer

The generic requirements of components are related to the embedding technology used, and shall be specified in the supply specification, including specific requirements on dimensions and tolerances.

Standard components can be used for embedding technologies using solder or conductive adhesive to realize electrical contacts. Specific embedding technologies, such as contacting the components by microvia, require components specially designed for that use.

The manufacturers of components for DES should provide information on the limiting conditions, e.g. sensitivity to pressure and mechanical forces, temperature, incompatibility with chemicals and ionic contaminations, as well as other stresses induced by embedding processes. Also, the thermal characteristic of the component under electrical load should be specified. The component supplier should also supply a material content data sheet in a format required by the submodule/board manufacturer.

4.2.4 Material manufacturer

Manufacturers of materials should be mindful of the limiting conditions and the characteristics of the components. In order to indicate that the material can't be specified for use with the components, either a purchase specification that reflects the limiting conditions and characteristics of the components in the frame of the upper and lower specification limits should be signed, or an early warning should be given.

4.2.5 Submodule manufacturer

The submodule manufacturer is responsible for selecting processes, materials and components that meet the specifications of the system manufacturer, but also ensure that no incompatibilities or reliability risks arise between the material, components and processes. The careful selection of materials, processes and components should be documented by purchase specifications signed by all suppliers that participate in the DES. Risks related to shipping, transportation, handling and assembly into the substrate shall be considered.

4.2.6 Board manufacturer

The board manufacturer shall provide design guidelines and a description of process capability. All processes needed for the selected embedding technology shall be qualified accordingly (see also Clause 7).

4.2.7 Assembly manufacturer

When processing the device embedded substrate (printed circuit board with devices embedded), the assembly manufacturer shall consider the allowable mechanical and thermal stresses as provided by the substrate manufacturer.

4.3 Traceability

Details and depth of traceability information shall be agreed between the involved partners at the beginning of a project. Traceability information, in form of a lot traveller or similar, should contain, among others, information on:

- components and material used,
- test and inspection records,
- indication of defective DES,
- test coupons (if required),
- manufacturing lot, date code or time stamp.

5 Safety aspects of base material and components

Safety requirements that apply to the base material and components are dependent on the final application and requirements of the system designer. These shall be communicated along the supply chain during the early stages of system development.

6 Design and structure of device embedded substrate

6.1 Basic rules for layer description

Built-up construction and terminology shall be established and aligned with suitable CAD systems used, taking into account the 3D structure of the device-embedded substrate.

6.2 Design for embedding and testability

For more details, see design guideline IEC TS 62878-2-3 and test guideline IEC TR 62878-2-2.

6.3 Safety aspects of design

The safety requirements of the design, e.g. clearance and creepage distances, need to be set and agreed between the system designer and suppliers.

7 Embedding technology

7.1 Basic technologies for embedding

For more details, see IEC TS 62878-2-1. Further information can be found in JPCA-EB01 and IPC 7092.

7.2 Basic requirements to embedding technology

7.2.1 Cleanliness of components, submodules and process

Surface properties and cleanliness shall be adapted to the processes. Related requirements shall be agreed between the involved partners.

EXAMPLE Surface roughness, ionic or organic contamination, oxidation.

7.2.2 ESD

If electrostatic sensitive devices are handled in the embedding process, an electrostatic control programme in accordance with IEC 61340-5-1 shall be developed, implemented and monitored. This programme covers all activities such as: manufacturing, processing, assembly, installation, packaging, labelling, servicing, testing, inspection or other handling of electrical or electronic parts, assemblies and equipment susceptible to damage by electrostatic discharges.

The level of protection against electrostatic discharge is determined by the most sensitive components to be processed.

For guidance, refer to IEC TR 61340-5-2.

7.2.3 Moisture sensitivity

When moisture-sensitive devices are handled in the embedding process, the instructions issued by the component manufacturers shall be followed [e.g. moisture sensitivity level (MSL), floor life, manufacturing exposure time, pre-drying].

For specification of the device-embedded substrate, the most moisture-sensitive component in its embedded stage shall be considered.