

INTERNATIONAL STANDARD

**Device embedding assembly technology –
Part 1: Generic specification for device embedded substrates**

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CONTENTS

FOREWORD.....	4
INTRODUCTION.....	6
1 Scope.....	7
2 Normative references	7
3 Terms and definitions	8
4 Value chain	8
4.1 System description.....	8
4.1.1 Generic design variants	8
4.1.2 Generic value chain	8
4.2 Elements of the value chain	9
4.2.1 General	9
4.2.2 System manufacturer.....	9
4.2.3 Components manufacturer.....	9
4.2.4 Material manufacturer.....	10
4.2.5 Submodule manufacturer.....	10
4.2.6 Board manufacturer	10
4.2.7 Assembly manufacturer	10
4.3 Traceability	10
5 Safety aspects of base material and components	10
6 Design and structure of device embedded substrate	11
6.1 Basic rules for layer description	11
6.2 Design for embedding and testability	11
6.3 Safety aspects of design	11
7 Embedding technology	11
7.1 Basic technologies for embedding.....	11
7.2 Basic requirements to embedding technology	11
7.2.1 Cleanliness of components, submodules and process	11
7.2.2 ESD.....	11
7.2.3 Moisture sensitivity	11
7.2.4 Defects	12
8 Tests and measuring methods	12
8.1 Standard atmospheric conditions	12
8.1.1 Standard atmospheric conditions for testing	12
8.1.2 Referee conditions.....	12
8.1.3 Reference conditions	13
8.2 Electrical performance tests.....	13
8.2.1 General	13
8.2.2 Electrical test levels.....	13
8.2.3 Protection of DES and test equipment	13
8.2.4 Accuracy of measurement	14
8.2.5 Test structures.....	15
8.2.6 Mechanical performance tests	15
8.2.7 Resistance to soldering heat.....	15
8.2.8 Solderability.....	16
8.2.9 Shock	16
8.2.10 Vibration (sinusoidal)	16

8.2.11	Resistance to solvents.....	16
8.3	Climatic performance tests.....	16
8.3.1	Dry heat	16
8.3.2	Cold.....	17
8.3.3	Damp heat, steady state.....	17
8.3.4	Change of temperature.....	17
9	Transportation, handling and packing material.....	18
9.1	Humidity / Temperature / Environmental protection	18
9.2	Mechanical protection	18
9.3	ESD.....	18
10	General requirements	18
	Bibliography.....	19
	Figure 1 – Value chain and interfaces	9
	Table 1 – Referee conditions	12

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 1: Generic specification for device embedded substrates

FOREWORD

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International Standard IEC 62878-1 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
91/1597/FDIS	91/1616/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

This document is a generic specification for device-embedded substrates fabricated by embedding discrete active and/or passive electronic devices into one or multiple inner layers of an organic substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Other special technologies for the realization of conductive or isolating structures and electronic components functions inside of substrates, like electronic modules or redistribution layers of integrated circuit packages are not covered by this document.

The device-embedded substrate can be used as a substrate to mount SMDs or THDs to form electronic circuits, as conductor and insulator layers can be formed after embedding electronic devices.

The purpose of this series of documents is to obtain common understanding in structures, test methods, design and fabrication processes and use of device-embedded substrate in the industry. These documents do not specify details of the manufacturing processes, design criteria and requirements, as those normally constitute intellectual property of the manufacturers and are very specific to the individual embedding technologies and applications.

Generic specification

The generic specification covers all subjects mainly common to device-embedded substrates for use in electronic equipment, such as terminology, methods of measurement and tests. Where the individual subjects require the prescription of conditions or parameters specific to the particular sub-family or type of embedded substrates, such prescriptions are required to be given by one of the subordinate specifications.

The numeric reference of the generic specification is IEC 62878-1.

Sectional and detail specifications (requirements to technology and components)

Sectional specifications cover all subjects additional to those given in the generic specification, which are specific to a defined sub-group of device-embedded substrate technologies. These subjects normally are preferred values for characteristics, additional test methods and relevant prescriptions for test methods given in the generic specification, prescriptions for sampling and for the preparation of specimens, recommended test severities and preferred acceptance criteria. The sectional specification also outlines the structure and scope of the test schedules that are to be applied in all subordinate detail specifications.

The numeric reference of the sectional and related detail specifications is IEC 62878-3-x.

Guidelines and supporting documentation

Supporting documentation and guidelines provide information in addition to the provisions of generic, sectional and detail specifications.

The numeric reference of supporting documentation and guidelines is IEC 62878-2-x.

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 1: Generic specification for device embedded substrates

1 Scope

This part of IEC 62878 specifies the generic requirements and test methods for device-embedded substrates. The basic test methods for printed board substrate materials and substrates themselves are specified in IEC 61189-3.

This part of IEC 62878 is applicable to device-embedded substrates fabricated by use of organic base material, which includes, for example, active or passive devices, discrete components formed in the fabrication process of electronic printed boards, and sheet-formed components.

The IEC 62878 series applies neither to the re-distribution layer (RDL) nor to electronic modules defined in IEC 62421.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-1, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60068-2-2, *Environmental testing – Part 2-2: Tests – Test B: Dry heat*

IEC 60068-2-6, *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60068-2-21, *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*

IEC 60068-2-27, *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*

IEC 60068-2-69, *Environmental testing – Part 2-69: Tests – Test Te/Tc: Solderability testing of electronic components and printed boards by the wetting balance (force measurement) method*

IEC 60068-2-78, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60194-2, *Printed board design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC 61340-5-3, *Electrostatics – Part 5-3: Protection of electronic devices from electrostatic phenomena – Properties and requirements classification for packaging intended for electrostatic discharge sensitive devices*

IEC 61760-4, *Surface mounting technology – Part 4: Classification, packaging, labelling and handling of moisture sensitive devices*

IEC 62137-1-4, *Surface mounting technology – Environmental and endurance test methods for surface mount solder joint – Part 1-4: Cyclic bending test*

IEC 62878-1-1, *Device embedded substrate – Part 1-1: Generic specification – Test methods*

IEC TS 62878-2-1, *Device embedded substrate – Part 2-1: Guidelines – General description of technology*

IEC TR 62878-2-2, *Device embedded substrate – Part 2-2: Guidelines – Electrical testing*

IEC TS 62878-2-3, *Device Embedded Substrate – Part 2-3: Guidelines – Design Guide*

IEC TS 62878-2-4, *Device Embedded Substrate – Part 2-4: Guidelines – Test element groups (TEG)*

J-STD 033, *Handling, Packing, Shipping, and Use of Moisture/Reflow and/or Process Sensitive Components*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

device-embedded substrate

DES

substrate in which one or more active devices (semiconductor device) and/or passive devices (e.g. resistor or capacitor) are formed using thick-film technology or by embedding them within the substrate

4 Value chain

4.1 System description

4.1.1 Generic design variants

Generic design variants are described in IEC TS 62878-2-1.

4.1.2 Generic value chain

The business model shown in Figure 1 shows the supply routes and communication along the value chain.