IEC 62148-19

Edition 1.0 2019-05

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Fibre optic active components and devices – Package and interface standards – Part 19: Photonic chip scale package

Composants et dispositifs actifs fibroniques – Normes de boîtier et d'interface – Partie 19: Boîtier à puce photonique

IEC 62148-19:2019-05(en-fr)

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CONTENTS

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FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – PACKAGE AND INTERFACE STANDARDS –

Part 19: Photonic chip scale package

FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
86C/1574/FDIS	86C/1586/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62148 series, published under the general title *Fibre optic active components and devices – Package and interface standards*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

A photonic chip scale package is used to convert electrical signals into optical signals and vice-versa. This document covers the physical interface for photonic chip scale packages. These modules are designed for use with free space optics or multiple channel optical fibre connectors.

FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – PACKAGE AND INTERFACE STANDARDS –

Part 19: Photonic chip scale package

1 Scope

This part of IEC 62148 covers the photonic chip scale package.

The purpose of this document is to specify adequately the physical requirements of optical transmitters and receivers that will enable mechanical interchangeability of transmitters and receivers.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62148-1, *Fibre optic active components and devices – Package and interface standards – Part 1: General and guidance*

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
photonic chip scale package
chip O/E and/or E/O convertor, where electrical I/Os and optical I/Os are also included

3.2 Abbreviated terms

CSP chip scale package
O/E optical to electrical
E/O electrical to optical
I/O input/output
SIG signal
TX transmitter
RX receiver
MOD optical modulator
LD laser diode

MMF multimode fibre
TIA transimpedance amplifier
PCB printed circuit board
PWB printed wiring board
PD photodiode

4 Classification

The photonic chip scale package specified in this document is classified as type 5 according to the definitions of IEC 62148-1.

5 Specification of photonic chip scale package

5.1 General

Clause 5 specifies the physical requirements of a photonic chip scale package that will enable mechanical interchangeability of modules complying with this document, both for the PCB and for any panel mounting requirement.

5.2 General block diagram (silicon photonics)

The block diagram for the photonic chip scale package is shown in Figure 1, which contains N channels of electrical inputs, M channels of electrical outputs, Q channels of optical outputs, and R channels of optical inputs.

The functions of electrical to optical (E/O) conversion or/and optical to electrical (O/E) conversion are provided by the package according to applications.

Channel numbers of electrical inputs N and optical outputs Q in E/O and optical inputs R and electrical outputs M in O/E are determined according to a multiplexing scheme such as wavelength multiplexing and serializer/deserializer.

Specific configurations for the photonic chip scale package are shown in Annex A.

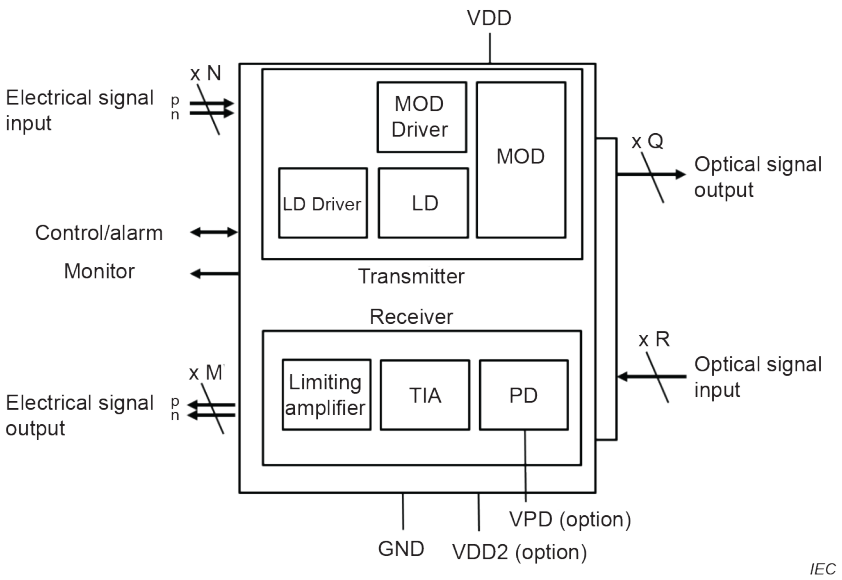


Figure 1 – General block diagram for photonic chip scale package

5.3 Electrical interface

5.3.1 General

The electrical interface in this document defines only the basic functionality of each terminal.

5.3.2 Numbering of electrical terminals

Electrical terminal numbering assignments are shown in Figure 2. The location of reference electrical terminal A1 is assigned at bottom left corner, and the direction of the package is decided by the position of the optical interface shifted to the left of centre, as shown in Figure 2.

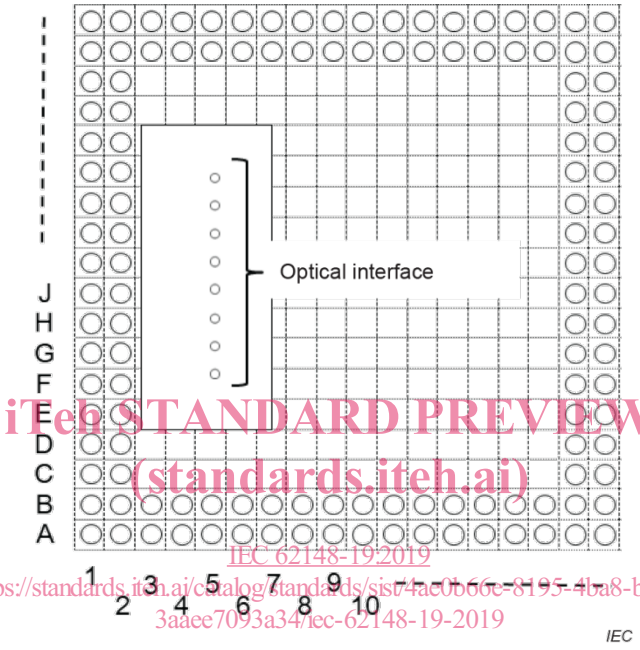


Figure 2 – Electrical terminal numbering assignment (top view)

5.4 Optical interface

5.4.1 General

The optical interface in this document defines only the basic functionality of each optical terminal. The channel spacing of optical interface has two options of 0,25 mm and 0,125 mm.

5.4.2 Free space optical beam condition

The optical output beam from a surface of the photonic chip scale package is coupled to an optical fibre or optical waveguide with free space optics, such as optical lenses or butt coupling, to have a specific coupling efficiency designed by each vendor.

Dimension of optical terminals and beam profiles are characterized in accordance with the vendor's specification.

5.5 Outline and footprint

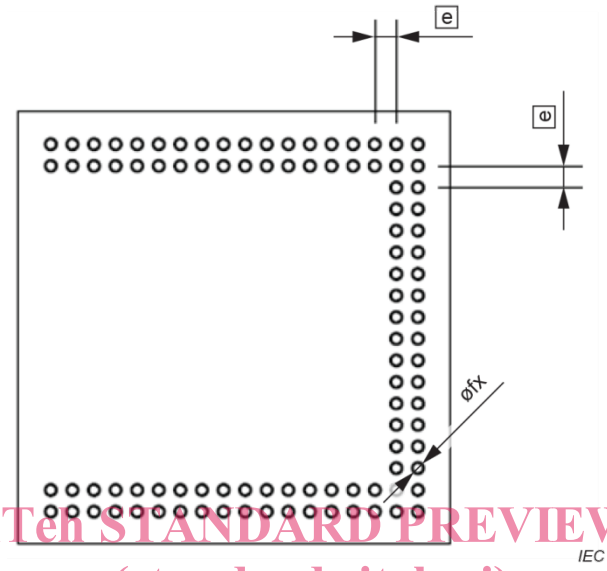
5.5.1 General

The footprint of the photonic chip scale package is determined by the number of channels of the optical transmitter and/or receiver and the dimensions and pitch of the electrical terminals. The electrical pad pitch and dimensions of the chip follow the general guidance for a chip scale package (IEC 62148-21).

Specific configurations for the photonic chip scale package are shown in Annex A.

5.5.2 Drawing of footprint

The recommended pattern layout for the PCB is shown in Figure 3, and informative electrical wiring for a high speed electrical interface is shown in Figure 4. The dimensions of recommended pattern layout for PCB are shown in Table 1.



NOTE e = 0,25 mm

Figure 3 – Recommended pattern layout for PCB

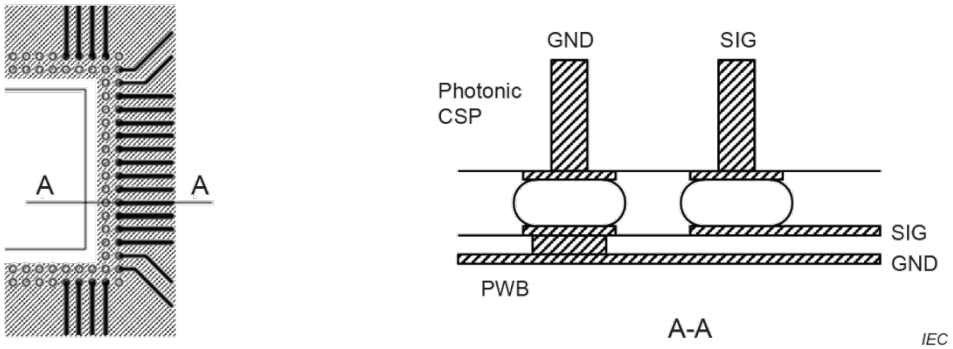


Figure 4 – Informative electrical strip line wiring for high speed electrical interface

Table 1 – Dimensions of recommended pattern layout for PCB

Reference	Dimensions mm	
	Minimum	Maximum
∅fx	0,13	0,17

Annex A
(normative)

Specific configurations

A.1 General

Specific configurations of chip scale package for multiple channel optical transmitter/receiver applications are described in Annex A. With options for optical channel spacing of 0,25 mm and 0,125 mm, alternatives of 4-channel transceiver (transmitter and receiver), 8ch transceiver, 12ch transmitter, and 12ch receiver are specified in Clauses A.2 to A.4, as listed in Table A.1.

Table A.1 – Specific configurations specified in Annex A

Configuration	Optical channel spacing	
	0,25 mm	0,125 mm
4ch transceiver	A.2	-
8ch transceiver	-	A.3
12ch transmitter/ 12ch receiver	-	A.4

A.2 4ch transceiver

A.2.1 Block diagram

The block diagram of a 4ch transceiver is shown in Figure A.1.

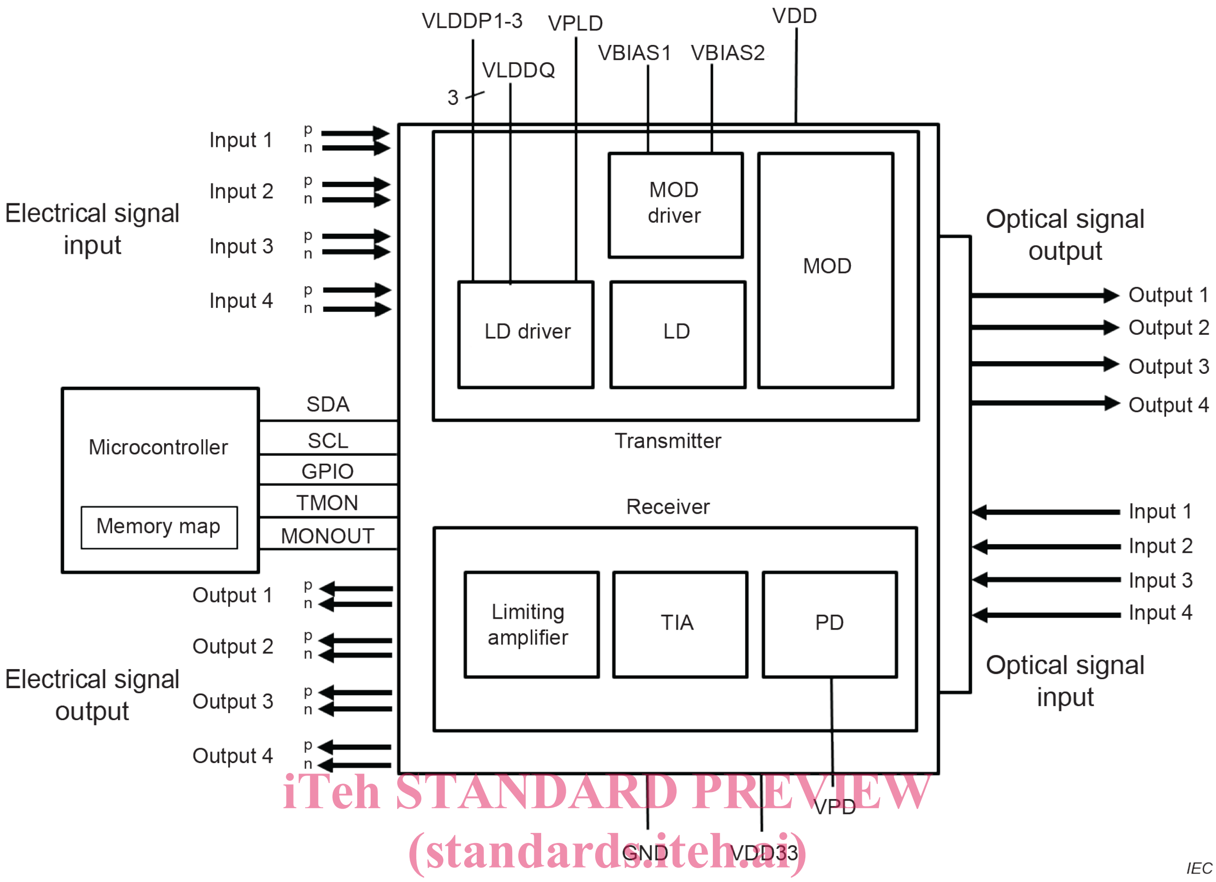


Figure A.1 – Block diagram for chip scale package of 4ch transceiver using silicon photonics chip with optional pads for LD control

A.2.2 Electrical terminal assignments

Electrical terminal numbering assignments are shown in Figure A.2. Electrical terminals in the outer two rows and columns (outer two lines) are used. The direction of the package is decided by the position of the optical interface shifted to the left of centre, as shown in Figure A.2. The terminal definitions are shown in Table A.2.

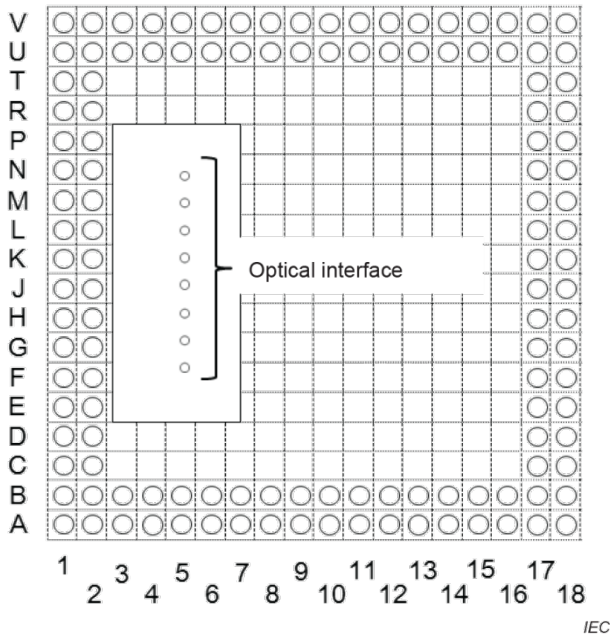


Figure A.2 – Electrical terminal numbering assignment (top view)

Table A.2 – Terminal function definitions for a 4ch transceiver

Terminal number	Symbol	Function
A1	GND	Ground
A2	GND	Ground
A3	GND	Ground
A4	VLDDQ	LD drive common
A5	VLDDP3	LD power supply 3 (external drive mode)
A6	VLDDP2	LD power supply 2 (external drive mode)
A7	VLDDP1	LD power supply 1 (external drive mode)
A8	GND	Ground
A9	VDD	Power supply
A10	GND	Ground
A11	VPLD	LD driver power supply
A12	VDD33	3,3 V power supply
A13	TMON	Temperature monitor output
A14	GND	Ground
A15	GND	Ground
A16	GND	Ground
A17	GND	Ground
A18	GND	Ground
B1	GND	Ground
B2	GND	Ground
B3	GND	Ground
B4	VLDDQ	LD drive common
B5	VLDDP3	LD power supply 3 (external drive mode)