IEC 62148-21

Edition 1.0 2019-03

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Fibre optic active components and devices – Package and interface standards – Part 21: Design guide of electrical interface of PIC packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA)

Composants et dispositifs actifs fibroniques – Normes de boîtier et d'interface – Partie 21: Guide de conception de l'interface électrique des boîtiers PIC utilisant des boîtiers matriciels à billes et à pas fins en silicium (S-FBGA) et des boîtiers matriciels à zone de contact plate et à pas fins en silicium (S-FLGA)

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FOREWORD

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International Standard IEC 62148-21 has been prepared by subcommittee 86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
86C/1571/FDIS	86C/1577/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62148 series, published under the general title *Fibre optic active components and devices – Package and interface standards*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – PACKAGE AND INTERFACE STANDARDS –

Part 21: Design guide of electrical interface of PIC packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA)

1 Scope

This part of IEC 62148 covers the design guide of the electrical interface for photonic integrated circuit (PIC) packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA). In this document, the electrical interface for the S-FBGA package is informative.

The purpose of this document is to specify adequately the electrical interface of PIC packages composed of optical transmitters and receivers that enable mechanical and electrical interchangeability of PIC packages.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication*

IEC TR 61931, *Fibre optic – Terminology*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731, IEC TR 61931 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
silicon fine-pitch ball grid array
S-FBGA
device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer balls on the dielectric layer(s), and outer balls with heights more than 0,1 mm

Note 1 to entry: This note only applies to the French language.

3.2
silicon fine-pitch land grid array
S-FLGA
device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer lands on the dielectric layer(s), and outer lands with heights of 0,1 mm or less

Note 1 to entry: This note only applies to the French language.

4 Terminal position numbering

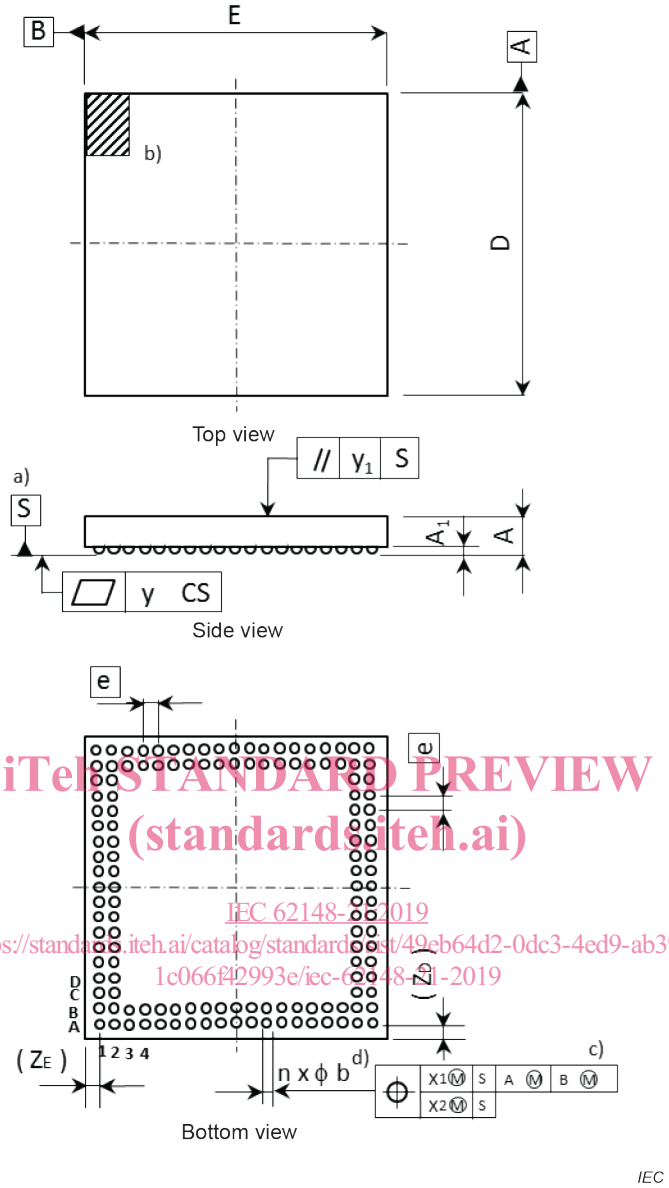
When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C…, AA, AB, etc.; whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, for example A1, B1. The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

5 Code of package nominal dimensions

A code of package nominal dimensions is defined as the combination of package length E and width D, which are shown to the second decimal place in millimetres.

6 Symbols and drawings

Figure 1 shows the dimensions of the package and the outline of the electrical interface for S-FBGA and S-FLGA. Figures 2 and 3 indicate the mechanical gauge drawing and its array of terminal existence area. Figure 2 shows the terminal existing area referred to Datum S, A and B. Figure 3 shows the terminal existing area referred to Datum S.



The letter symbols used in the figure are listed and described in Table 1.

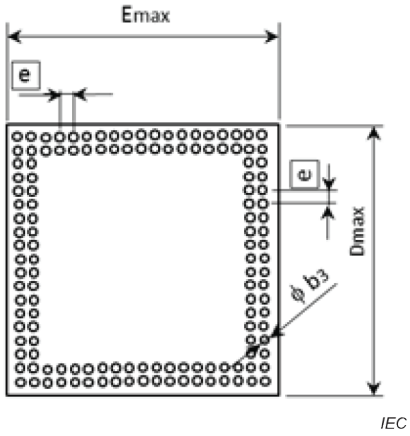
a) Datum S is the seating plane on which a package stays.

b) The hatched zone is an index-marking area indicating A1 corner.

c) True positional tolerances of terminals x1 and x2 are applied to all terminals.

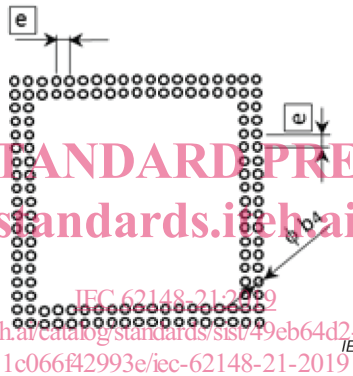
d) The terminal diameter b is the maximum diameter of the ball as measured in a plane parallel to the seating plane.

Figure 1 – S-FBGA and S-FLGA outline



The letter symbols used in the figure are listed and described in Table 1.

Figure 2 – Mechanical gauge drawing



The letter symbols used in the figure are listed and described in Table 1.

Figure 3 – Array of terminal-existence areas

7 Dimensions and tolerances

Table 1 specifies the tolerance of each symbol parameter; Table 2 and Table 3 indicate the options of D, E, M_D and M_E.

Table 1 – Dimensions and tolerances

Term	Symbol	Specification	Recommended value	Notes
Code of package nominal dimensions	D X E	Code of package nominal dimension is defined as the combination of package width D and package length E, which are shown in the second decimal place	-	-
Package width	D	Package width is shown in the second decimal place Package width D_{nom} Minimum 0,50 Maximum 10,00 Tolerance V_D ±0,05		V_D denotes tolerance.
Package length	E	Package length is shown in the second decimal place Package length E_{nom} Minimum 0,50 Maximum 10,00 Tolerance V_E ±0,05		V_E denotes tolerance
Profile height	A	When A is ≤ 0,65, the tolerance of nominal height is ±0,07. When 0,8 ≤ A ≤ 1,0, the tolerance of nominal height is ±0,10. A shall not exceed 1,0.		A includes package warpage and tilt allowances.
Stand-off height	A1	1) For S-FBGA (informative) e: 0,3 bnom: 0,2 min 0,1 nom 0,15 max 0,2 For low stand-off S-FBGA A1 ≤ 0,20 2) For S-FLGA e: 0,25 A1 ≤ 0,10		
Terminal pitch	e	1) For S-FBGA (informative) 0,3 2) For S-FLGA 0,25		
Terminal diameter	b	1) For S-FBGA (informative) e: 0,3 min 0,17 nom 0,20 max 0,23 2) For S-FLGA e: 0,25 min 0,10 nom 0,13 max 0,16		

Datum-based positional tolerance of terminals	x1	x1 = 0,08		
Relative positional tolerance of terminals	x2	1) For S-FBGA (informative) e:0,3 x2 = 0,03 2) For S-FLGA e:0,25 x2 = 0,03		
Coplanarity	y	1) For S-FBGA (informative) e:0,3 y = 0,05 2) For S-FLGA e:0,25 y = 0,05		
Parallelism of the top surface	y1	y1 = 0,08		
Number of terminals	n	n = M_D x M_E (M_D – 1) x M_E M_D x (M_E – 1) (M_D – 1) x (M_E – 1) $M_E \leq (E - b_{max} - V_E - x1 - x2)/e + 1$ $M_D \leq (D - b_{max} - V_D - x1 - x2)/e + 1$		Numbers of matrices in M_E and M_D are shown in Table 3.
Maximum matrix size in length	M_E			
Maximum matrix size in width	M_D			
Overhang dimension in width	Z_D	$Z_D = [D_{nom} - (M_D - 1) \times e] / 2$	-	Reference value
Overhang dimension in length	Z_E	$Z_E = [E_{nom} - (M_E - 1) \times e] / 2$	-	Reference value
Datum-defined Terminal-existence area	b3	b3 = bmax + x1		
Relative Terminal existence area	b4	b4 = bmax + x2		
NOTE Dimensions are in millimetres.				