IEC 63011-1

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INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Integrated circuits – Three dimensional integrated circuits –
Part 1: Terminology

Circuits intégrés – Circuits intégrés tridimensionnels –
Partie 1: Terminologie

IEC 63011-1:2018-11(en-fr)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 1: Terminology

FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1060/FDIS	47A/1064/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63011 series, published under the general title *Integrated Circuits – Three dimensional integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

High performance electrical system requires a massive data exchange between processing integrated circuit (IC) and storage IC. Stacked multiple ICs with a large number of vertical interconnects among dies are an innovative way of providing higher data transfer rate among dies. In addition to bumps, metal pillars, or metal pads which are traditional ways of interconnection between dies, through-silicon vias enable to configure the integration of three or more dies. The integration environment of multichip IC is significantly different from that of the integration on a printed circuit board. This document describes definitions pertaining to the multichip ICs.

INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 1: Terminology

1 Scope

This part of IEC 63011 provides definitions pertaining to multichip integrated circuits, as vertically stacked dies using through-silicon vias (TSVs) or micro bumps. Terms and definitions related to the fabrication and test of the multichip integrated circuits are also provided.

2 Normative reference

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1 General

The general terms listed below relate to the secondary integration method in vertical direction using integrated circuits fabricated on a horizontal surface of semiconductor.

3.1.1
interposer
electrical interface that connects one socket or connection to another

Note 1 to entry: The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection

3.1.2
multichip interconnect technology
technology that allows for the vertical stacking of layers of basic electronic components which are connected using an interconnect fabric are as follows:

Note 1 to entry: "Basic electronic components" are elementary circuit devices such as transistors, diodes, resistors, capacitors and inductors.

Note 2 to entry: A special case of multichip interconnect technology is the interposer structures that may only contain interconnect layers, although in many cases other basic electronic components (in particular decoupling capacitors) may be embedded into the interposer.

3.1.3
3-D bonding
process that joins two die or wafer surfaces together multiple surfaces mechanically or electrically

EXAMPLE: Die-to-die, die-to-wafer, wafer-to-wafer

3.1.4
3-D stacking
3-D bonding operation that assumes electrical interconnects between the two devices

3.1.5
3-D packaging
3-D integration of multiple dies using wire bonding, package-on-package stacking, or embedding in printed circuit boards

3.1.6
3-D wafer-level-packaging
3-D WLP
3-D integration using wafer level packaging technologies, performed after wafer fabrication, which consists of flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging, and fan-out reconstructed wafer chip-scale packaging

Note 1 to entry: This note applies to the French language only.

3.1.7
redistribution layer
RDL
extra metal layer on a chip that makes the IO pads of an integrated circuit available in other locations

Note 1 to entry: This note applies to the French language only.

3.1.8
system in package
SIP
integration of multiple dies, packages, or mixture of them as system in a package

Note 1 to entry: This note applies to the French language only.

3.1.9
3-D stacked integrated circuit
3-D approach using direct interconnects without wire bonding between integrated circuits of multiple dies

Note 1 to entry: The 3-D stack uses a sequence of alternating front-end (devices) and back-end (interconnect) layers.

3.1.10
3-D integrated circuit
3-D IC
3-D approach using direct stacking of active devices

Note 1 to entry: Interconnects are on the local on-chip interconnect levels. The 3-D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack.

Note 2 to entry: This note applies to the French language only.

3.2 Test method in 3D environment

3.2.1
package stack
integrated circuit packaging method to combine vertically discrete logic and memory ball grid array (BGA) packages

Note 1 to entry: Two or more packages are installed atop each other.

3.2.2
package-on-package
POP
package in which multiple packages are enclosed

Note 1 to entry: This note applies to the French language only.

3.2.3
multi-chip-package
MCP
package in which multiple dies are stacked vertically or placed side-by-side

Note 1 to entry: This note applies to the French language only.

3.2.4
die stack
chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit

3.2.5
contacting die stack
chip in which two or more layers of active electronic components are integrated and signals between multiple layers are transferred via physical and electrical contacts

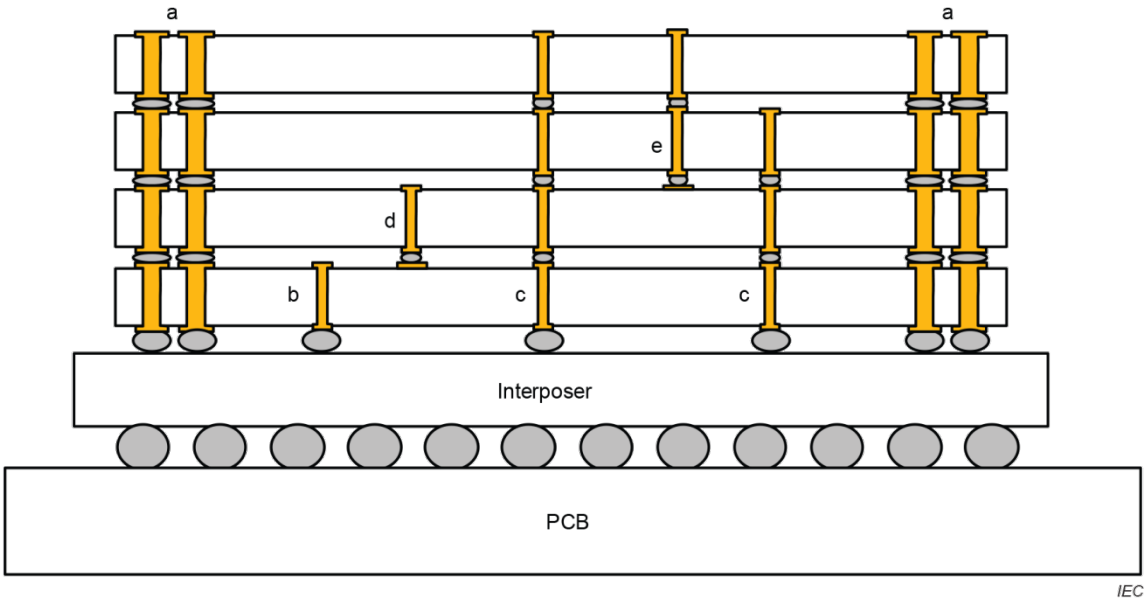
3.2.6
bump
stud of metal protruded on the surface of die to provide the physical and electrical contact

3.2.7
micro bump
small size bump to make an electrical contact between two dies

3.2.8
flip chip
die mounted with face down

3.2.9
through-silicon via
TSV
vertical interconnect access passing completely through a silicon wafer or die

Note 1 to entry: Examples of TSVs are shown in Figure 1.



Key

a power TSV;

b single drop signal TSV;

c multiple drop signal TSV;

d inter-die jumper;

e stacked inter-die jumper.

Figure 1 – Examples of TSVs

3.2.10
power TSV
TSV intended to deliver power from one layer to another layer of stacked silicon wafers or dies

Note 1 to entry: Examples are shown in Figure 1.

3.2.11
single drop signal TSV
TSV intended to deliver electric signals from one layer to another layer of stacked silicon wafers or dies

Note 1 to entry: An example is shown in Figure 1.

3.2.12
multiple drop signal TSV
TSV intended to deliver electric signals from one layer to multiple layers of stacked silicon wafers or dies

Note 1 to entry: An example is shown in Figure 1.

3.2.13
inter-die jumper
TSV bridging circuits between adjacent two layers of stacked dies, that is not connected to the output pin of the package

Note 1 to entry: An example is shown in Figure 1.