SLOVENSKI STANDARD
SIST EN 60191-6-12:2011

01-oktober-2011

Standardizacija mehanskih lastnosti polprevodniških elementov - 6-12. del: Splošna pravila za pripravo tehničnih risb okrovov polprevodniških elementov za površinsko montažo - Vodilo za konstruiranje drobne rastrske mreže priključkov v ravnini (FLGA)

Mechanical standardization of semiconductor devices - Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch land grid array (FLGA)

Mechanische Normung von Halbleiterbauelementen - Teil 6-12: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für Feinraster-Land-Grid-Array (FLGA)

Normalisation mécanique des dispositifs à semiconducteurs - Partie 6-12: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface - Guide de conception pour les boîtiers FLGA

Ta slovenski standard je istoveten z: **EN 60191-6-12:2011**

ICS:

01.100.25	Risbe s področja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

SIST EN 60191-6-12:2011 **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60191-6-12

August 2011

ICS 31.080.01

Supersedes EN 60191-6-12:2002

English version

Mechanical standardization of semiconductor devices - Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guidelines for fine-pitch land grid array (FLGA)

(IEC 60191-6-12:2011)

Normalisation mécanique des dispositifs à semiconducteurs -
Partie 6-12: Règles générales pour la préparation des dessins d'encombrement des boîtiers des dispositifs à semiconducteurs à montage en surface - Lignes directrices de conception pour les boîtiers matriciels à plots et à pas fins (FLGA)
(CEI 60191-6-12:2011)

Mechanische Normung von Halbleiterbauelementen -
Teil 6-12: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für Feinraster-Land-Grid-Array (FLGA)
(IEC 60191-6-12:2011)

This European Standard was approved by CENELEC on 2011-07-13. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47D/784/CDV, future edition 2 of IEC 60191-6-12, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-12 on 2011-07-13.

This European Standard supersedes EN 60191-6-12:2002.

EN 60191-6-12:2011 includes the following significant changes with respect to EN 60191-6-12:2002:

a) scope is expanded so that this standard include the square type FLGA. The title of this standard has been changed accordingly: “Rectangular type” has been deleted from the title;

b) ball pitch of 0,3 mm has been added;

c) datum is changed from the body datum to the ball datum;

d) combination lists of *D, E,* M_D, and M_E have been revised.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2012-04-13

– latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2014-07-13

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-12:2011 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191	Series	Mechanical standardization of semiconductor devices	EN 60191	Series
IEC 60191-6	-	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages	EN 60191-6	-

IEC 60191-6-12

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INTERNATIONAL STANDARD

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colour inside

Mechanical standardization of semiconductor devices – Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guidelines for fine-pitch land grid array (FLGA)

Normalisation mécanique des dispositifs à semiconducteurs – Partie 6-12: Règles générales pour la préparation des dessins d'encombrement des boîtiers des dispositifs à semiconducteurs à montage en surface – Lignes directrices de conception pour les boîtiers matriciels à plots et à pas fins (FLGA)

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FOREWORD

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International Standard IEC 60191-6-12 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This second edition of IEC 60191-6-12 cancels and replaces the first edition, published in 2002 and constitutes a technical revision. This edition includes the following significant changes with respect to the previous edition:

a) scope is expanded so that this standard include the square type FLGA. The title of this standard has been changed accordingly: "Rectangular type" has been deleted from the title.
b) ball pitch of 0,3 mm has been added;
c) datum is changed from the body datum to the ball datum;
d) combination lists of D, E, M_D, and M_E have been revised.

The text of this standard is based on the following documents:

CDV	Report on voting
47D/784/CDV	47D/795/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guidelines for fine-pitch land grid array (FLGA)

1 Scope

This part of IEC 60191 provides standard outline drawings, dimensions, and recommended variations for all fine-pitch land grid array packages (FLGA) with terminal pitch of 0,8 mm or less.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191(all parts), *Mechanical standardization of semiconductor devices*

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*

3 Terms and definitions

For the purposes of this document, the terms and definitions given IEC 60191 series and the following apply.

3.1
fine-pitch land grid array
FLGA
package with metal lands on one side of a substrate in a matrix of at least three rows and three columns on a pitch of 0,8 mm or less, wherein the maximum standoff height is 0,10 mm or less

NOTE Terminals may be missing from some row-column intersections.

3.2
flange-type FLGA
FLGA with a package outline (length, width) defined by a package flange part, mostly substrate, extending outward beyond the perimeter of a molded part or of a flip-chip-bonded part

NOTE Flange-type FLGA, shown in Figure 1, is generally cut by singulation press, thus resulting in larger dimensional errors than the singulation by dicing saw