IEC 62878-2-5

Edition 1.0 2019-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

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Device embedding assembly technology – Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate

Technologie d'ensemble avec appareil(s) intégré(s) – Partie 2-5: Lignes directrices – Mise en œuvre d'un format de données 3D pour un substrat avec appareil(s) intégré(s)

IEC 62878-2-5:2019-09 (en-fr)

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate

FOREWORD

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International Standard IEC 62878-2-5 has been prepared by IEC technical committee 91: Electronics assembly technology.

This bilingual version (2020-01) corresponds to the monolingual English version, published in 2019-09.

This first edition cancels and replaces IEC PAS 62878-2-5 published in 2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the title has been changed to "Implementation of a 3D data format for device embedded substrate" from "Requirements of design date format for device embedded substrate";
b) the scope of this implementation has changed to not include SiPs.

The text of this International Standard is based on the following documents:

CDV	Report on voting
91/1557/CDV	91/1589/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate

1 Scope

This part of IEC 62878 specifies requirements based on XML schema that represents a design data format for device embedded substrate, which is a board comprising embedded active and passive devices whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material.

This data format is to be used for simulation (e.g. stress, thermal, EMC), tooling, manufacturing, assembly, and inspection requirements. Furthermore, the data format is used for transferring information among printed board designers, printed board simulation engineer, manufacturers, and assemblers.

This part of IEC 62878 applies to substrates using organic material. It neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as M-type business model in IEC 62421.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
artwork information
information that shows a SiP not included in net and figure data in board (symbol mark, inside of SiP, mould, spacer, remarks, etc.)

3.2
board information
total information of a device-embedded substrate, including embedded devices

3.3
chip stack
package of semiconductor chips stacked vertically

3.4
clearance
area around a through-hole where there is no conductor to prevent electrical connection between a large conductor area, such as that of a power supply or a ground and a plated through-hole

3.5
computer-aided manufacturing
CAM
interactive use of computer systems, programs, and procedures in various phases of a manufacturing process wherein the decision-making activity rests with the human operator and a computer provides the data manipulation functions

3.6
computer-aided design
CAD
interactive use of computer systems, programs, and procedures in the design process wherein the decision-making activity rests with the human operator and a computer provides the data manipulation function

3.7
DXF
data format for AutoCAD

Note 1 to entry: AutoCAD is the trade name of a product supplied by Autodesk®. This information is given for the convenience of users of this document and does not constitute an endorsement by IEC of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Note 2 to entry: It generally means a type of data format to draw figures using CAD board data.

3.8
design document
documentation of information necessary in circuit board design

3.9
device arrangement information
information that includes the position, the shape and attributes of the embedding device included in the net information

3.10
device embedded substrate
substrate in which an active device(s) (semiconductor device) and/or passive device(s) (e.g. resistor, capacitor) is formed using thick-film technology or by embedding it within the substrate

3.11
FLIP chip
FC
leadless monolithic circuit element structure that electrically and mechanically interconnects to a printed board by conductive bumps

3.12
Gerber
type of data format that consists of aperture selection and operation commands and dimensions in X- and Y-coordinates

Note 1 to entry: The data is generally used to direct a photo-plotter in generating photo-plotted artwork.

Note 2 to entry: Gerber is the trade name of a product supplied by Ucamco. This information is given for the convenience of users of this document and does not constitute an endorsement by IEC of the product named. Equivalent products may be used if they can be shown to lead to the same results.

3.13
interposer
material placed between two surfaces giving electrical insulation, redistribution of electrical connections, mechanical strength and/or controlled mechanical and thermal separation between the two surfaces

Note 1 to entry: An interposer may be used as a means for redistributing electrical connections and/or allowing for different thermal expansions between adjacent surfaces.

3.14
land
pad
portion of a conductive pattern usually used for the connection and/or attachment of components

3.15
land definition
maintainance of a shape of specific land, pad, solder resist and others

3.16
layer definition
combination of physical information of shape and construction and logic information giving design and production units

3.17
layer map
map showing the relation between devices and the board, the devices being arranged on the board

3.18
library
database of design information based on a design document, to be used in board CAD

3.19
logical layer
layer that can be arbitrarily formed in the event that it is difficult to physically express a layer in a design

Note 1 to entry: It is possible to relate it to a physical layer.

Note 2 to entry: It is different from the layers in a multi-layer substrate.

3.20
micro-electro-mechanical system
MEMS
system integrating micro-machine, mechanical elements, sensor, actuator, and electronic circuit into one module

3.21
net information
device pin construction and wiring pattern in this PAS

3.22
package information
shapes of board and devices when they have package shape patterns in this document

3.23
PoP
package on package
single or multiple package(s) mounted on a package of a single chip or multiple chips as single package

3.24
physical layer
layer consisting of a physical layer construction and structure

3.25
port information
information of figures and names of external terminals of a device or a substrate with terminals

3.26
structure
total structure of a device embedded substrate and/or surface device mounted to the substrate

3.27
SiP
system in a package
multi-chip package (MCP) that performs a system function

3.28
thermal land
heat energy may leak to outside of a land/through-hole when a device is soldered on a large pattern such as power supply or ground. A cut is often made around such a soldering point to prevent thermal dissipation

3.29
through silicon via
TSV
hole made in a silicon chip and filled with metal to electrically connect upper and lower side of the chip for 3D stacking package

3.30
via definition
via that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material

3.31
virtual layer
name of the layer connecting conductor layers when a device is embedded

Note 1 to entry: It corresponds to the connection point of a device terminal specified in IEC TS 62678-2-3.

3.32
wire bonding
WB
micro-bonding between a die and base material, lead frame, etc.

4 Data definition

4.1 Flow chart design of device embedded substrate

Figure 1 shows the design flow of a device embedded substrate. The design data can be directly sent to a board manufacturing system using this format, or can be converted to CAM data and then be used in production. The data contain 3D information of coordinates and shapes of devices used. It is possible to check the status of device embedding in a board, and also make it a common knowledge in production know-how of a production line.

This file format describes the detailed 3D information of the following electronic circuit boards, including device embedded substrate and SiP (system in package), and makes it possible to use necessary information from the stage of design to the fabrication of products.

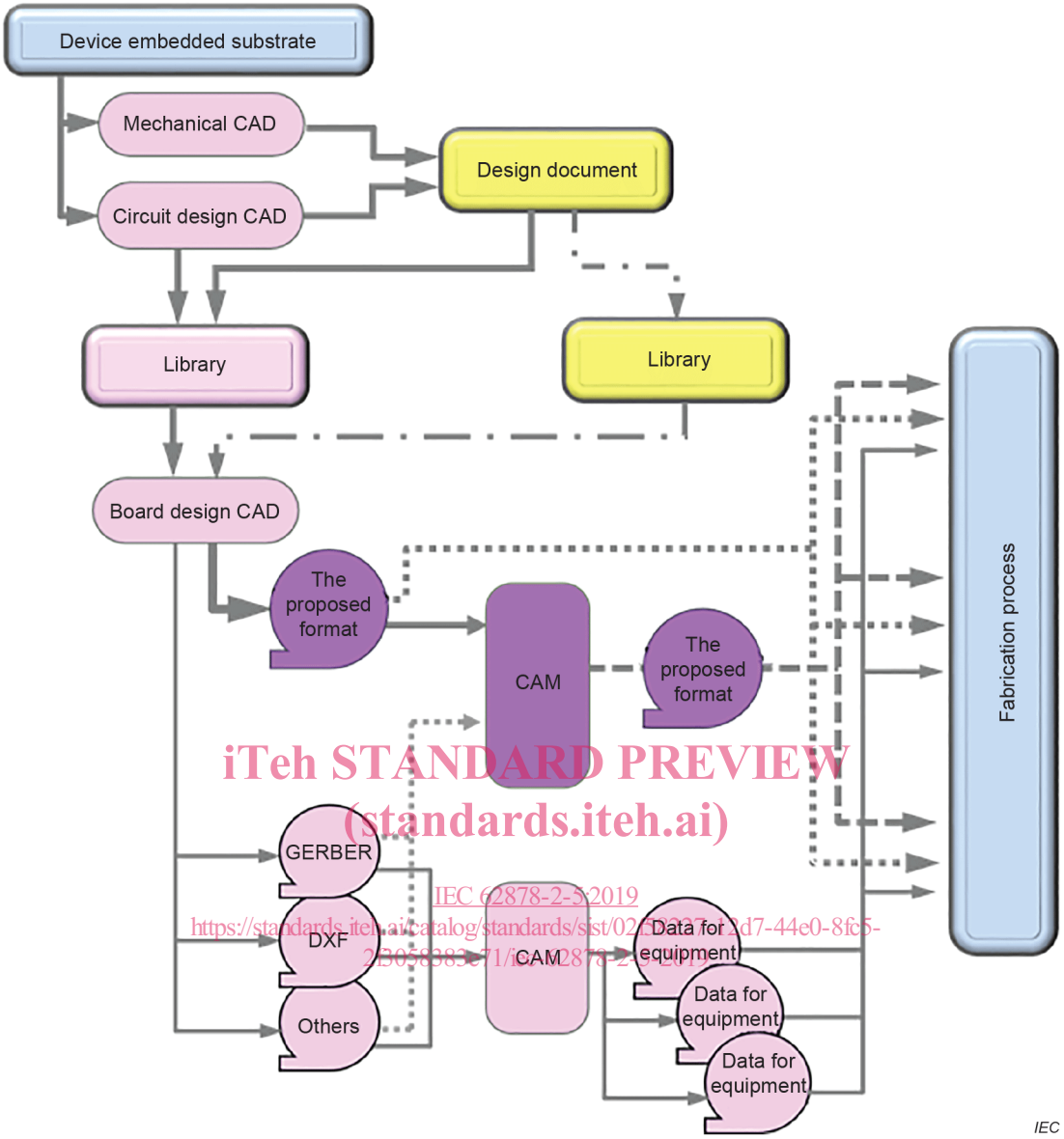
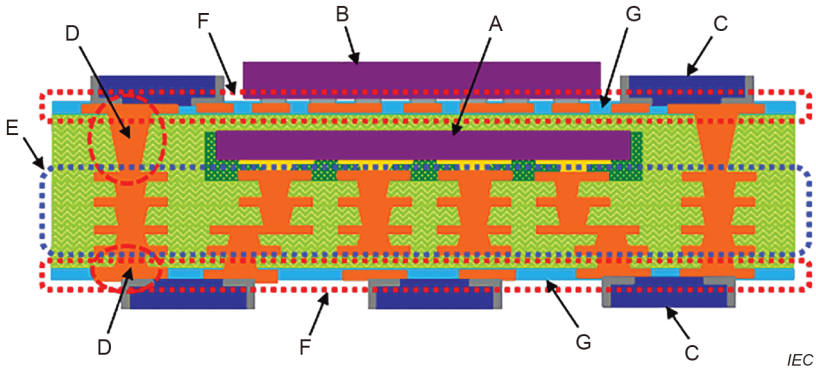


Figure 1 – Flow chart of design of device embedded substrate

4.2 Applicable range

4.2.1 Product

It is possible to maintain the following design information of a device embedded substrate as shown in Figure 2.



A	Embedded active device	E	Inner pattern
B	Surface mounted active device	F	Surface pattern
C	Surface mounted passive device	G	Solder resist
D	Layer connecting via		

Figure 2 – General structure of device embedded substrate

4.2.2 Process

The format describes maintained and available information of each stage in production as described in Table 1:

1) design,
2) simulation,
3) substrate fabrication,
4) device embedding,
5) test.

Table 1 – Required information

Process	Holding data	Available data
Design	Circuit Components Shape of the board Board structure Design/Production rule (for check)	Limited condition Net list
Simulation	Circuit Characteristics of components Board properties (materials) Board structure Art work	Electrical properties Thermal properties Mechanical properties Electronic properties Additional information in production
Substrate fabrication	Art work Drilling Symbol marks Panel format	Equipment Additional information in production
Device embedding	Component shape Embedding position Interconnection terminals Symbol marks	Equipment Relative positions of component Component list
Test	Art work Component shape Component position Terminal information Marks	Electrical test equipment Video image inspection

4.3 Features

4.3.1 General

The data format has the following characteristics:

1) can contain the structure of the device embedded substrate specified in IEC TS 62678-2-3;
2) can contain information of SiP in general (chip stack, PoP TSV, wire bonding, FLIP chip, interposer, etc.);
3) holds design data of terminal positions of embedding device in a virtual layer specified in IEC TS 62678-2-3;
4) information on the internal structure of devices such as SiP, which cannot be described as a structure of a device embedded substrate and of a terminal structure as 3D design data;
5) seamless keeping of design data of devices having different levels, such as SiPs, and of embedding substrate.

4.3.2 Device embedded substrate structure

It is possible to keep and illustrate the 3D structure of the device embedded substrate as shown in Figure 3. It is also possible to check its 3D structure.