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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Integrated circuits – Three dimensional integrated circuits – Part 3: Model and measurement conditions of through-silicon via

Circuits intégrés – Circuits intégrés tridimensionnels – Partie 3: Modèle et conditions de mesure des trous de liaison à travers le silicium

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IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

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International Standard IEC 63011-3 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1057/FDIS	47A/1063/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63011 series, under the general title *Integrated circuits – Three dimensional integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

The embedded system implementation such as digital consumer and mobile devices is a history of functional integration and power reduction for faster and smaller. At the beginning, the embedded system was developed by various digital ASIC chips to implement required functions. They were then integrated on one chip as a system on chip (SoC), which includes application processor and peripheral I/F logic, such as PCIe, SATA, USB, and DDRx memory controller. Because required performance and image resolution is growing, SoC has embedded many functions through adopting advanced semiconductor technology.

Since advanced semiconductor technology is complicated and its development cost is higher, the application is limited to use only for a few products. Those SoC's cost is not appropriate for all embedded systems. Multi-chip implementation is a way to solve this issue. It implements very large logic gate on the separated SoC and ASIC logic chips, connecting each other. This multi-chip interconnection technique provides also implementation of heterogeneous technology VLSI chips.

This document is focused to interconnect methodology to implement multi-chip VLSI for three-dimensional integrated circuit. Thanks to through-silicon via (TSV) and micro bump interconnect technology; the wire number between VLSI can be tremendously wider. It also allows to connect chips with on-chip bus interconnection, which has several thousand signal connections.

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

1 Scope

This part of IEC 63011 specifies a reference model of through-silicon via (TSV) electrical characteristics required for an interface design in three dimensional integrated circuit (3-D IC) to transmit and receive digital data and measurement conditions for resistance and capacitance to specify TSV characteristics in 3-D IC.

3-D IC specifications covered by this document are the following:

- application: digital consumer and mobile;
- operating voltage: 0,1 V to 5,0 V,
- operating frequency: less than 2,0 GHz.

This document does not describe the equipment for the measurement. Figure 1 describes a typical case of multi-chip interconnect system discussed in this document.

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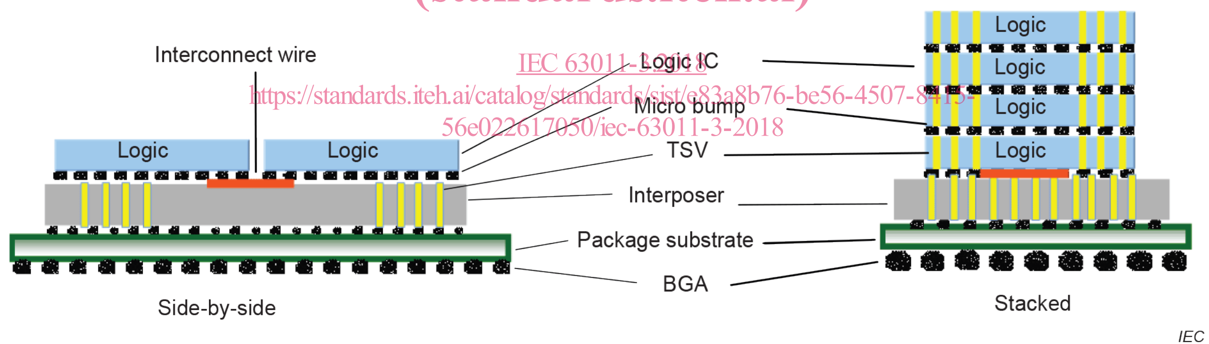

Figure 1 – Reference of a multi-chip interconnect system

Power devices, RF devices and micro-electromechanical systems (MEMS) are not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63011-1, *Integrated circuits – Three dimensional integrated circuits – Part 1: Terminology*

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 63011-1 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
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3.2 Abbreviated terms

3-D IC	three-dimensional integrated circuit
ASIC	application specific integrated circuit
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SoC	system on chip
TSV	through-silicon via
VLSI	very large scale integration

4 Measurement conditions to specify TSV characteristics

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4.1 Supply chain and TSV circuit model

3-D IC supply chain employing the TSV circuit model is shown in Figure 2. Foundry manufacturers of logic chip and 3-D stacking provide the TSV model. The circuit model is determined based on an actual experimental result.

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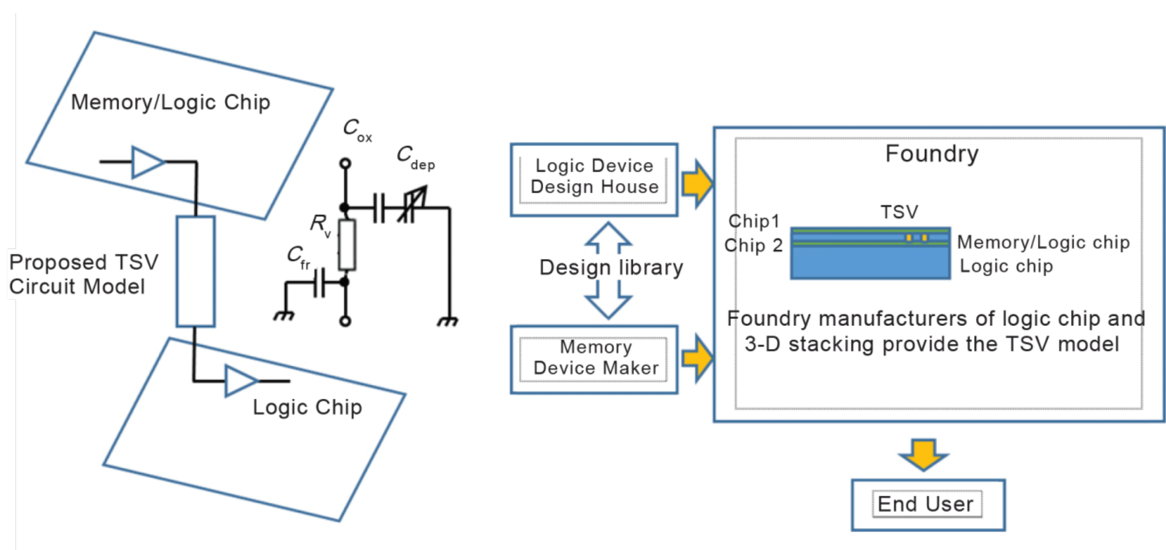

Figure 2 – 3-D IC Supply chain model

4.2 Reference model of TSV electrical characteristics

Reference model of TSV electrical characteristics shown in Figure 3 is composed of a capacitance (C_v) and a resistance (R_v). C_v is the total capacitance and consists of capacitance of oxide layer (C_{ox}), capacitance by depletion layer (C_{dep}) and fringe capacitance (C_{fr}). C_{ox} and C_{dep} are capacitances between the TSV and the semiconductor substrate and dependent on the voltage applied to the TSV since depletion layer exists. C_{fr} is a fringe capacitance between a bump and the semiconductor substrate. The node of C_{dep} is connected to the ground through the substrate. When the interval of TSV is very short, coupling model is recommended. Table 1 shows a policy for model standardization. Circuit definition explains the view of proposed model. The device structure is the structure which will be the requisite in the case of using the proposed model. Measurement condition explains device structure and operating conditions for measurement. The parameters of the TSV model are derived from TSV and its surrounding structure. An example of a typical concept is shown in Annex A.

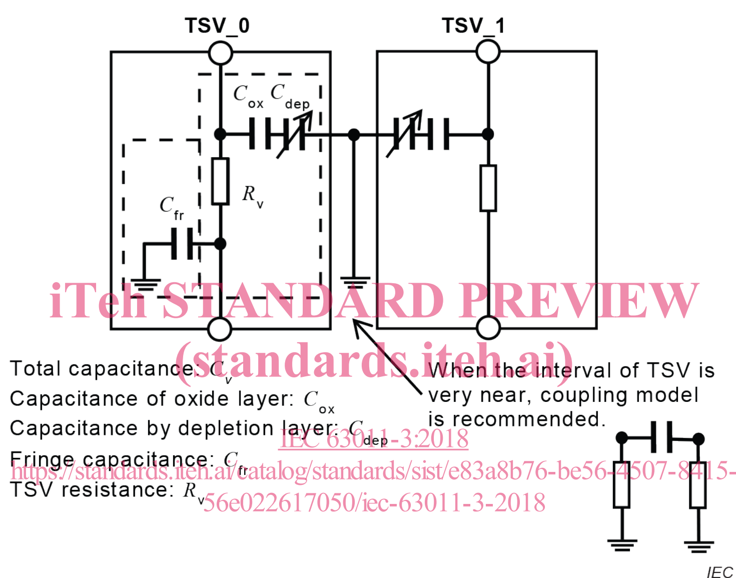

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Figure 3 – TSV electrical characteristic model

Table 1 – Policy for model standardization

Item	Subitem	Policy
Circuit definition	Parameter	Resistance is defined with average value. Capacitance is defined by a waveform. Fringe capacitance is removable Inductance is not included because of little influence.
	Model for every application	No definition
Device structure	Surrounding TSV	No definition When the interval of TSV is very short, coupling model is recommended.
	Semiconductor substrate power supply	Substrate is connected to the ground. The defined TSV circuit model is inapplicable when substrate isn't connected to power supply.
	Semiconductor substrate	P type
Measurement condition	Structure	TSV array There is difference from single TSV and array TSVs.
	Frequency	Frequency dependence of capacitance is measured.
	Voltage	Voltage dependence of capacitance is measured.

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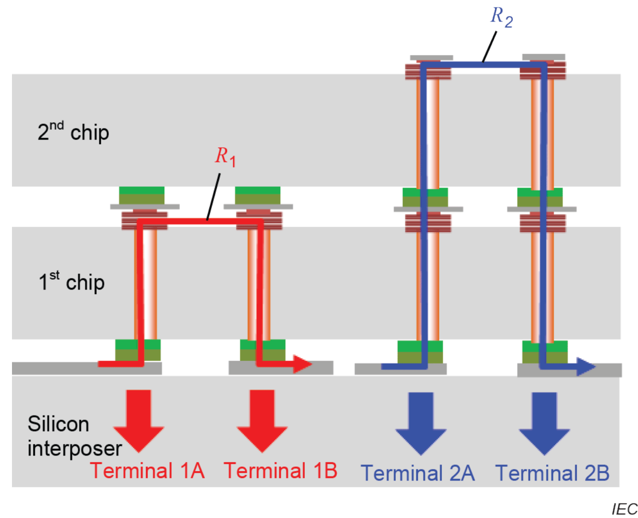
4.3 Measurement conditions to specify TSV electrical characteristics

4.3.1 General

The electrical characteristics of the TSV shall be measured with the defined conditions.

4.3.2 Resistance measurement

TSV resistance (R_v), consisting of bulk resistances of LSI interconnect, TSV, bumps and their contact resistances, is obtained by four point measurement. A constant current (I) is supplied via current supply wirings connecting to terminal 1A and terminal 1B, and the generated voltage (V) between wirings connecting to the terminals is measured by voltmeter as shown in Figure 4. According to Ohm's law, a pair resistance for the first chip (R_1) is defined as V/I. Based on the same setup, a resistance for the first chip and the second chip (R_2) is obtained. TSV resistance (R_v) is defined as (R_2-R_1)/2. This method is only valid when the second chip is essentially the same as the first chip. To minimize measurement error, the voltage measurement wiring should be connected as close as possible.



TSV resistance (R_v) is defined as $R_v = R_2 - R_1/2$, where R_1 is the first chip, and R_2 is the second chip.

Figure 4 – Resistance measurement method

4.3.3 Capacitance measurement

TSV capacitance (C_v) is obtained by electrical impedance measurement. Overall capacitance (C_1) between terminal 1A and terminal 1B is measured by an impedance meter as a function of signal frequency (f) and DC voltage (V_{dc}) as shown in Figure 5. This capacitance (C_1) is composed of TSV capacitance (C_v) and the parasitic capacitance (C_2) caused by the measurement wiring and experimental setup. Therefore, TSV capacitance (C_v) is given by $C_1 - C_2$. Parasitic capacitance (C_2) between terminal 2A and terminal 2B is obtained by impedance measurement for a measurement structure having neither TSV nor bump. Using TSV array is recommended to reduce parasitic capacitance.

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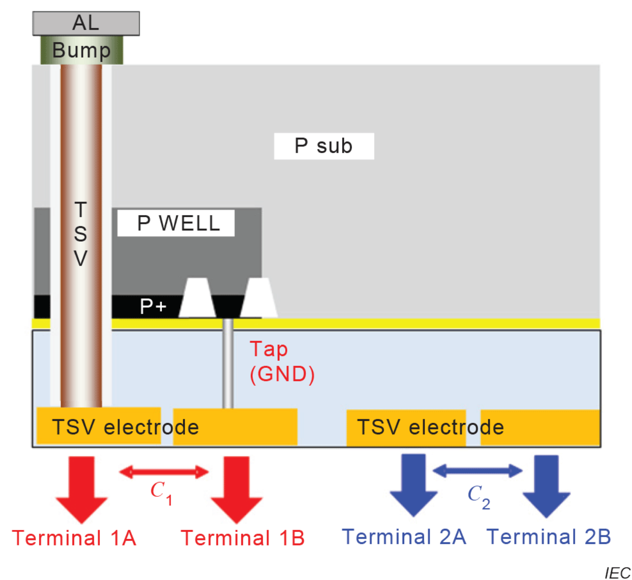

TSV capacitance (C_v) is given by $C_1 - C_2$, where C_1 is the capacitance, and C_2 is the parasitic capacitance.

Figure 5 – Capacitance measurement method