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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 4: Damp heat, steady state, highly accelerated stress test (HAST)

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 4: Essai continu fortement accéléré de contrainte de chaleur humide (HAST)

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 4: Damp heat, steady state, highly accelerated stress test (HAST)

FOREWORD

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International Standard IEC 60749-4 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2002. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) clarification of requirements for temperature, relative humidity and duration detailed in Table 1;
b) recommendations that current limiting resistor(s) be placed in the test set-up to prevent test board or DUT damage;
c) allowance of additional time-to-test delay or return-to-stress delay.

This bilingual version (2019-09) corresponds to the monolingual English version, published in 2017-03.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2346/FDIS	47/2371/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 4: Damp heat, steady state, highly accelerated stress test (HAST)

1 Scope

This part of IEC 60749 provides a highly accelerated temperature and humidity stress test (HAST) for the purpose of evaluating the reliability of non-hermetic packaged semiconductor devices in humid environments.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-5, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady state temperature humidity bias life test*

3 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 HAST test – General remarks

The HAST test employs severe conditions of temperature, humidity and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the “85/85” steady-state temperature humidity bias life test, IEC 60749-5. As such the test method may be selected from IEC 60749-5 or from this test method. When both test methods are performed, test results of the 85 °C/85 % RH steady-state temperature humidity bias life test, IEC 60749-5, take priority over HAST.

This test method shall be considered destructive.

5 Test apparatus

5.1 Test apparatus requirements

The test requires a pressure chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

5.2 Controlled conditions

The chamber shall be capable of providing controlled conditions of pressure, temperature and relative humidity during ramp-up to and ramp-down from the specified test conditions.

5.3 Temperature profile

A permanent record of the temperature profile for each test cycle is recommended so that the validity of the stress can be verified.

5.4 Devices under stress

Devices under stress shall be mounted in such a way that temperature gradients are minimized. Devices under stress shall be no closer than 3 cm from internal chamber surfaces, and shall not be subjected to direct radiant heat from heaters. Boards on which devices are mounted should be oriented to minimize interference with vapour circulation.

5.5 Minimize release of contamination

Care shall be exercised in the choice of board and socket materials, to minimize release of contamination and to minimize degradation due to corrosion and other mechanisms.

5.6 Ionic contamination

Ionic contamination of the test apparatus (card cage, test boards, sockets, wiring storage containers, etc.) shall be controlled to avoid test artefacts.

5.7 De-ionized water

De-ionized water with a minimum resistivity of 1×10^4 Ωm at room temperature shall be used.

6 Test conditions

6.1 Test conditions requirements

Test conditions consist of a temperature, relative humidity, and duration in conjunction with an electrical bias configuration specific to the device. Unless otherwise required by the detailed specification the test conditions shall be selected from Table 1.

Table 1 – Temperature, relative humidity and duration requirements

Temperature[a] (dry bulb) °C	Relative humidity[a] %	Temperature[b] (wet bulb) °C	Vapour pressure[b] kPa	Duration[c] h
130 ± 2	85 ± 5	124,7	230	96 ($^{+2}_{0}$)
110 ± 2	85 ± 5	105,2	122	264 ($^{+2}_{0}$)
For parts that reach absorption equilibrium in 24 h or less, the HAST test is equivalent to at least 1 000 h at 85 °C/85 % RH. For parts that require more than 24 h to reach equilibrium at the specified HAST condition, the time should be extended to allow parts to reach equilibrium. Caution: For plastic-encapsulated micro-circuits, it is known that moisture reduces the effective glass transition temperature of the moulding compound. Stress temperatures above the effective glass transition temperature can lead to failure mechanisms unrelated to standard 85 °C/85 % RH stress.				
[a] Tolerances apply to the entire useable test area. [b] For information only. [c] The test conditions are to be applied continuously except during any interim readouts when devices should be returned to stress within the time specified in 7.6. The 96 h and 264 h test durations were selected to be at least equivalent 1 000 h of 85 °C/85 % RH stress using a worst case activation energy of E_a = 0,65 eV.				

6.2 Biasing guidelines

Apply bias according to the following guidelines:

a) Minimize power dissipation.

b) Alternate pin bias as much as possible.

c) Distribute potential differences across chip metallization as much as possible.

d) Maximize voltage within operating range.

NOTE The priority of the above guidelines depends on mechanism and specific device characteristics.

e) Either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

1) Continuous bias

The DC bias shall be applied continuously. Continuous bias is more severe than cycled bias when the die temperature is ≤10 °C higher than the chamber ambient temperature or, if the die temperature is not known when the heat dissipation of the DUT is less than 200 mW. If the heat dissipation of the DUT exceeds 200 mW, then the die temperature should be calculated. If the die temperature exceeds the chamber ambient temperature by more than 5 °C, then the die temperature rise above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

2) Cycled bias

The DC voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10 °C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with a 50 % duty cycle is optimal for most plastic encapsulated microcircuits. The period of the cycled stress should be ≤ 2 h for packages ≥ 2 mm in thickness and ≤ 30 min for packages < 2 mm in thickness. The die temperature, as calculated on the basis of the known thermal impedance and dissipation should be quoted with the results whenever it exceeds the chamber ambient by 5 °C or more.

6.3 Choosing and reporting

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the die temperature exceeds the chamber ambient temperature, are summarized in Table 2.

Table 2 – Bias and reporting requirements

ΔT_{ja}	Cyclical bias	Report ΔT_{ja}
ΔT_{ja} < 5 °C, or power per DUT <200 mW	No	No
(ΔT_{ja} ≥ 5 °C or power per DUT ≥200 mW), and ΔT_{ja} < 10 °C	No	Yes
ΔT_{ja} ≥ 10 °C	Yes	Yes

7 Procedure

7.1 Test device mounting

The test devices shall be mounted in a manner that exposes them to a specified condition of temperature and humidity with a specified electrical biasing condition. Exposure of devices to excessively hot, dry ambient or conditions that result in condensation on devices and electrical fixtures shall be avoided, particularly during ramp-up and ramp-down.

7.2 Ramp-up

The time to reach stable temperature and relative humidity conditions shall be less than 3 h. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times, and that the rate of ramp up shall not be faster than a rate which ensures that the temperature of any DUT does not lag below the wet bulb temperature. The dry- and wet-bulb temperature set points shall be maintained so that the relative humidity is not less than 50 % after significant heating begins. In a dry laboratory, the chamber ambient may initially be drier than this.

7.3 Ramp-down

The first part of ramp-down to a slightly positive gauge pressure (a wet bulb temperature of about 104 °C) shall be long enough to avoid test artefacts due to rapid depressurization but shall not exceed 3 h. The second part of ramp-down from a wet bulb temperature of 104 °C to room temperature shall occur with the chamber vented. There is no time restriction and forced cooling of the vessel is permitted. Condensation on devices shall be avoided in both parts of the ramp down by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times. Ramp-down should maintain the moisture content of the moulding compound encapsulating the die. Therefore, the relative humidity shall not be less than 50 % during the first part of the ramp down (see 7.2).

7.4 Test clock

The test clock starts when the temperature and relative humidity reach the set points and stops at the beginning of ramp-down.

7.5 Bias

Bias application during ramp-up and ramp-down is optional. Bias should be verified after devices are loaded, prior to the start of the test clock. Bias should also be verified after the test clock stops, but before devices are removed from the chamber.

It is recommended that current limiting resistor(s) be placed in the test set-up to prevent test board or DUT damage in case a short circuit develops during the test.

7.6 Readout

An electrical test shall be performed not later than 48 h after the end of ramp-down.

For intermediate readouts, devices should be returned to stress within 96 h of the end of ramp down. The rate of moisture loss from devices after removal from the chamber can be reduced by placing the devices in sealed moisture barrier bags (without desiccant). When devices are placed in sealed bags, the “test window clock” runs at one-third of the rate of devices exposed to the laboratory ambient. Thus the test window can be extended to as much as 144 h and the time to return to stress to as much as 288 h by enclosing the devices in moisture-proof bags.

The electrical test parameters should be chosen to preserve any defect (i.e. by limiting the applied test current).

Additional time-to-test delay or return-to-stress delay may be allowed if justified by technical data.

7.7 Handling

Suitable hand-covering shall be used to handle devices, boards and fixtures. Contamination control shall be exercised in any highly-accelerated moisture stress test.

7.8 Calibration records

Calibration records shall verify that, for steady state conditions and maximum thermal mass loading, test conditions are maintained within the tolerances specified.

8 Failure criteria

A device shall be considered as having failed the highly accelerated temperature and humidity stress test if parametric limits are exceeded, or if functionality cannot be demonstrated under nominal and worst-case conditions as specified in the applicable procurement document or data sheet.

9 Safety

The equipment manufacturer's recommendations and local safety regulations shall be followed.