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TECHNICAL REPORT

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Documentation on design automation subjects – Mathematical algorithm hardware description languages for system level modeling and verification (HDLMath)

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DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – MATHEMATICAL ALGORITHM HARDWARE DESCRIPTION LANGUAGES FOR SYSTEM LEVEL MODELING AND VERIFICATION (HDLMath)

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IEC 63051, which is a Technical Report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
91/1349/DTR	91/1396/RVC

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
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INTRODUCTION

Around the world, engineers in industries such as electronics and automobiles are developing many kinds of systems and products. However, these are developed based on conventional design processes and suffer from many design problems and long design times. Because the laws of nature can be expressed mathematically, mathematics is a good algorithmic method for the description and modeling of such systems. Mathematical modeling is also an important approach for both solving problems and visualizing the abstract concepts involved.

System LSI (Large Scale Integration) can be described at three levels of complexity as follows:

1) The the algorithmic level, which specifies only the algorithm used by the hardware for the problem solution;
2) the register transfer level, in which the registers are system elements and the data transfer between these registers is specified according to some rule;
3) the circuit level, where gates and flip-flops are replaced by the circuit elements such as transistors, diodes, resistors, etc.

For levels 2) and 3), VHDL (IEC 61691-1-1:2011 [1][1]) and SystemVerilog (IEC 62530:2011[2]) have already been standardized by the IEC and IEEE and have been in practical use for over twenty years.

For level 1), System C is able to describe hardware systems at the behavioral level.

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The purpose of this document is to accelerate the standardization of a mathematical algorithm description language (HDLMath). HDLMath will be used to describe and verify the entire behavior of systems and/or products using mathematical algorithms of electronic systems. It is a higher level language than conventional HDL (Hardware Description Language) languages such as VHDL and SystemVerilog.

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HDLMath and its design environment can support the design of many domains and applications as indicated in Table 1.

Table 1 – Examples of mathematics applications

Mathematics	Application examples
Complex numbers	Resistors, inductors, capacitors, power engineering, analysis of electric and magnetic fields, digital signal processing, image processing
Matrices and determinants	Electrical networks, computer graphics, image analysis
Laplace transforms	Circuits, power systems (generators), feedback loops
Statistics and probability	Failure rates for semiconductor devices, behavior of semiconductor materials, image analysis, data compression, digital communications techniques, error correction
Vector and trigonometry	Oscillating waves (circuits, signal processing), electric and magnetic fields, design of power generating equipment, radio frequency (RF) systems and antenna design
Differentiation and integration	Calculation of currents in a circuit, wave propagation, design of semiconductors, image analyses, design of firing circuits
Functions, polynomial, linear equations, logarithms, Euclidean geometry	Curve fitting, fuel cell design, traffic modeling, power analysis, stress analysis, determining the size and shape of parts, software design, computer graphics

[1] Numbers in square brackets refer to the Bibliography.

Recently, several HDLMath languages have already been used to design the mathematical algorithms in electronic systems. MATLAB/SIMULINK is one such popular design environment for the design and verification of various system behaviors. FinSimMath has been proposed and put to practical use by several groups to design and verify mathematical algorithms in ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). System C-AMS is mainly for analog circuit design and is an extension of the System C standardized by the IEEE and IEC. It is capable of describing mathematical algorithms using additional C-code extensions. IEC TR 62856:2013 [3] (BVDL, or Bird's-eye View of Design Languages) describes the features of existing design languages, as well as listing the requirements for enhancing design languages and for developing new ones.

Another purpose of this document is to add HDLMath to BVDL as a system modeling language. This document describes nine functional requirements for an HDLMath and compares current HDLMath languages from a design viewpoint. It is intended to accelerate the standardization of a mathematical algorithm design language and to establish a good system modeling environment in the world.

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DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – MATHEMATICAL ALGORITHM HARDWARE DESCRIPTION LANGUAGES FOR SYSTEM LEVEL MODELING AND VERIFICATION (HDLMath)

1 Scope

A hardware description language provides a means to describe the behavior of a system precisely and concisely. This document describes the main functional requirements for an HDLMath language and compares existing HDLMath languages from the viewpoint of designers. It is intended to accelerate the standardization of a mathematical algorithm design language and to help establish a new and good system modeling and verification environment.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

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3 Terms and definitions

No terms and definitions are listed in this document.

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- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 Definition and positioning of HDLMath

4.1 General

HDLMath is defined as a language for describing and verifying the behavior of an entire system or product using mathematical algorithms.

IEC TR 62856:2013 (BVDL) describes the features of existing design languages used in the design processes applied to the development of System-on-Chip (SoC) devices, which range from system level design, IP block creation and analog block design, to SoC design implementation and verification. HDLMath will cover system level design in the BVDL schema.

4.2 Current HDLMaths

Currently, there are three kinds of language for these design environments: HDLMath1, HDLMath2, and HDLMath3.

HDLMath1 is a kind of high-level language that has an interactive environment for numerical computation, visualization, and programming. It is able to analyze data, develop algorithms, and create models and applications using the language, tools, and built-in mathematical functions. It features the following:

a) a block diagram environment for multi-domain simulation and model-based design;

b) simulation, automatic code generation, and continuous test and verification of embedded systems.

HDLMath2 is motivated by the need for mathematical modeling within the Verilog language. Its features are as follows:

- no explicit conversion functions are necessary;
- support for runtime changes of formats, including the number of bits of the various fields;
- data in multi-dimensional arrays that are easy to access globally.

The language is designed to support a large number of mathematical system tasks, and provides access to information regarding the occurrence of overflows, underflows, maximum number of bits needed, cumulative error, etc.

HDLMath3 is a language mainly to support analog design. It allows networks of analog parts such as resistors, capacitors, etc., to be defined. The simulator extracts the differential equations corresponding to the network of analog parts and solves them based on initial conditions and using a timestep provided by the user. It is able to handle blocks that are modeled mathematically and written at the C/C++ level. However, the mathematical capabilities in math.h (a kind of C function library) are limited at the low level of C/C++ and not at the high levels found in HDLMath1 or HDLMath2.

4.3 Design abstraction level of HDLMath

Figure 1 shows the number of lines of code for several small examples written using HDLMath1 and HDLMath2. It also shows the length of the C-code generated automatically from an HDLMath1 description. The number of lines of C-code is several hundred times larger than that of the HDLMath descriptions. The figure indicates how HDLMath languages can be used to design at a higher level of design abstraction and hence how design productivity is higher than C level design.

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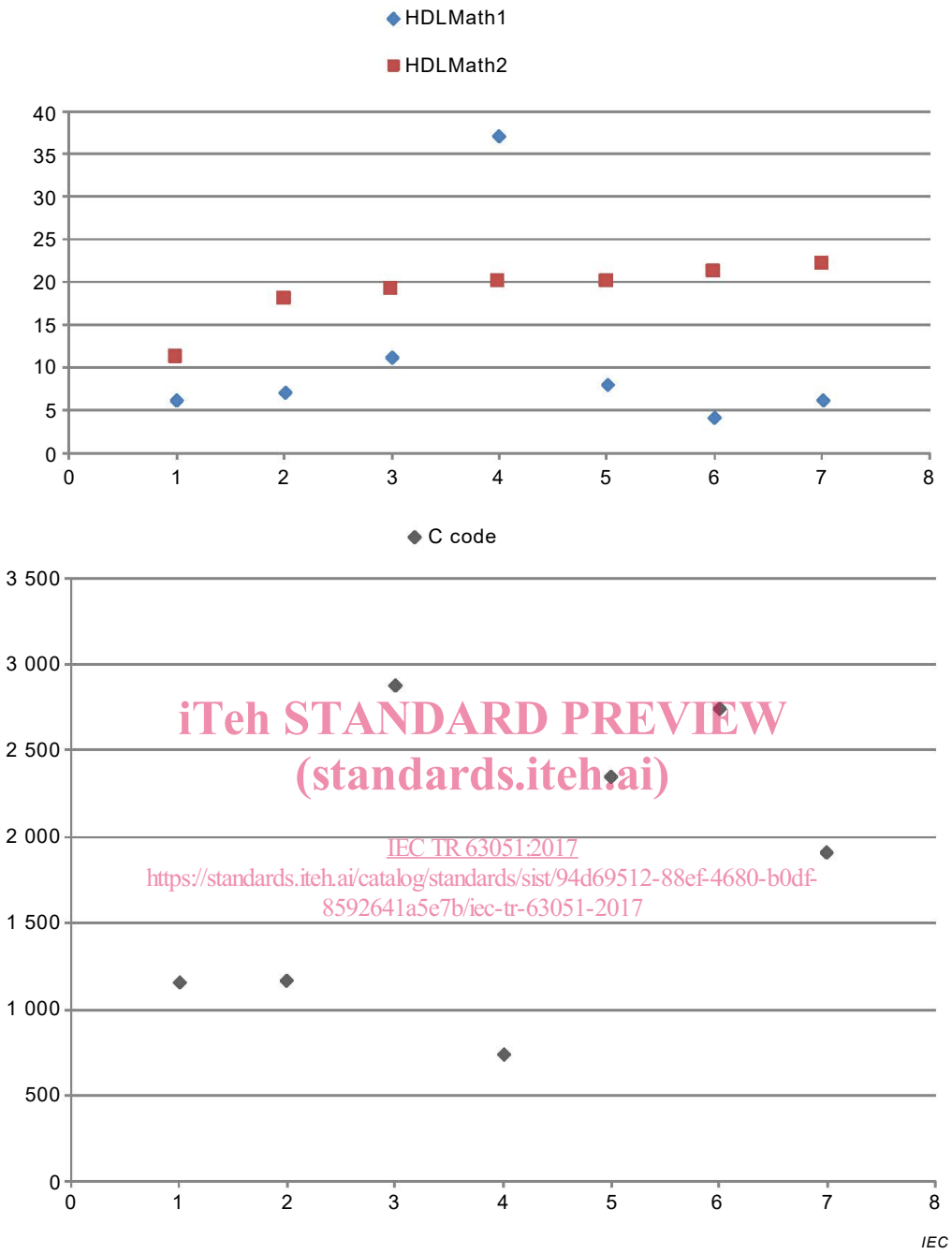

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Figure 1 – Numbers of description lines

5 Functional requirements of HDLMath

5.1 General

When designing mathematical algorithms for system level modeling with an HDLMath, the HDLMath shall cover the following functional requirements in order to achieve utmost precision.

5.2 Mathematical expressions

The mathematical operators +, -, *, **, and / shall be applicable to any combination of the following operand and result formats: arbitrary-precision fixed-point, arbitrary-precision floating-point, integer, real, register, and constants. Trigonometric and hyperbolic (direct and inverse) functions shall be supported for any precision. Power, logarithm, and square root