

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Mechanical and climatic test methods –
Part 6: Storage at high temperature**

**Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques –
Partie 6: Stockage à haute température**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –
MECHANICAL AND CLIMATIC TEST METHODS –****Part 6: Storage at high temperature**

FOREWORD

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International Standard IEC 60749-6 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2002. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) additional test conditions;
- b) clarification of the applicability of test conditions.

This bilingual version (2019-09) corresponds to the monolingual English version, published in 2017-03.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2347/FDIS	47/2372/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 6: Storage at high temperature

1 Scope

The purpose of this part of IEC 60749 is to test and determine the effect on all solid state electronic devices of storage at elevated temperature without electrical stress applied. This test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure methods and time-to-failure of solid state electronic devices, including non-volatile memory devices (data-retention failure mechanisms). This test is considered non-destructive but should preferably be used for device qualification. If such devices are used for delivery, the effects of this highly accelerated stress test will need to be evaluated.

Thermally activated failure mechanisms are modelled using the Arrhenius equation for acceleration, and guidance on the selection of test temperatures and durations can be found in IEC 60749-43.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

4 Test apparatus

The controlled temperature chamber required for this test shall be capable of maintaining the test temperature within the tolerances specified in Table 1. Electrical equipment shall be capable of performing the appropriate measurements for the devices being tested, including writing and verifying the required data retention pattern(s) for non-volatile memories.

5 Procedure

5.1 Test conditions

The devices under test (DUT) shall be subject to continuous storage (except when there is a requirement in the applicable procurement document to return the DUTs to room ambient for interim electrical measurements) at one of the temperatures specified in Table 1. Qualification and reliability monitoring test conditions typically require a test duration of 1 000 °C₀⁺²⁴ at test temperature B of Table 1. Other test conditions can be used as appropriate.

Caution should be exercised when selecting an accelerating test condition since the accelerated temperature may exceed the capabilities of the device and materials, thereby inducing (overstress) failures that would not occur under normal use conditions. As a minimum, the following items should be taken into consideration.

- 1) the maximum rated storage temperature T_{stg} , max;
- 2) the melting point and degradation of metals present, especially solder;
- 3) the temperature limitations of silicon devices; for example, charge loss in non-volatile memories;
- 4) package degradation (e.g. glass transition temperature and thermal stability of any polymeric materials);
- 5) moisture rating of the package (see IEC 60749-20).

Table 1 – High temperature storage conditions

Condition	Temperature °C $\begin{matrix} +10 \\ 0 \end{matrix}$
A	125
B	150
C	175
D	200
E	250
F	300

5.2 Measurements

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Unless otherwise specified, interim and final electrical measurements shall be completed within 168 h after removal of the devices from the specified test conditions. Intermediate measurements are optional unless otherwise specified. The time window need not be met if verification data for a given technology is provided. If the final readpoint time window is exceeded then the units may be restressed for the same amount of time that the window is exceeded. For non-volatile memories, the data specified data retention pattern shall be written initially, and then subsequently verified without re-writing.

The electrical measurements shall consist of parametric and functional tests specified in the applicable procurement document.

NOTE If interim measurements are considered necessary they can be chosen from:

$$24h \begin{matrix} +8 \\ 0 \end{matrix} \quad 48h \begin{matrix} +8 \\ 0 \end{matrix} \quad 96h \begin{matrix} +8 \\ 0 \end{matrix} \quad 168h \begin{matrix} +8 \\ 0 \end{matrix} \quad 500h \begin{matrix} +12 \\ 0 \end{matrix}$$

5.3 Failure criteria

A device will be considered a high temperature storage failure if parametric limits are exceeded, or if functionality cannot be demonstrated under nominal and worst-case conditions, specified in the relevant procurement document. For non-volatile memories, the specified data retention pattern shall be verified before and after storage. A margin test may be used to detect data retention degradation.

Mechanical damage, such as cracking of the package, will be considered a failure. Cosmetic package defects and degradation of lead finish, or solderability are not considered failure criteria.

6 Summary

The following details shall be specified in the relevant specification:

- a) electrical measurements (see 5.2);
- b) sample size;
- c) test temperature, if other than specified (see 5.1, Table 1);
- d) test duration, if other 1 000 h (see 5.1);
- e) intermediate measurements, if required (see 5.2);
- f) Nonvolatile memory data retention pattern (for appropriate devices) (see 5.3).

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Bibliography

IEC 60749-20, *Semiconductor devices – Mechanical and climatic test methods – Part 20: Resistance of plastic encapsulated SMDs to the combined effect of moisture and soldering heat*

IEC 60749-43¹, *Semiconductor devices– Mechanical and climatic test methods – Part 43: Guidelines for IC reliability qualification plans*

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¹ Under preparation. Stage at the time of publication: IEC/CDV 60749-43:2016.

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