

# SLOVENSKI STANDARD

## SIST EN 60191-4:2014

01-maj-2014

Nadomešča:

SIST EN 60191-4:2002

SIST EN 60191-4:2002/A1:2005

SIST EN 60191-4:2002/A2:2005

---

**Standardizacija mehanskih lastnosti polprevodniških elementov - 4. del: Kodirni sistem in klasifikacija oblik okrovov polprevodniških elementov (IEC 60191-4:2013)**

Mechanical standardization of semiconductor devices - Part 4: Coding system and classification into forms of package outlines for semiconductor device packages

(standards.iteh.ai)

Mechanische Normung von Halbleiterbauelementen - Teil 4: Codierungssystem für Gehäuse und Eingruppierung der Gehäuse nach der Gehäuseform für Halbleiterbauelemente

<https://standards.iteh.ai/catalog/standards/sist/fl1f5eae-f6a8-4954-b8e9-54d38c79aef0/sist-en-60191-4-2014>

Normalisation mécanique des dispositifs à semiconducteurs - Partie 4: Système de codification et classification en formes des boîtiers pour dispositifs à semiconducteurs

**Ta slovenski standard je istoveten z: EN 60191-4:2014**

---

**ICS:**

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
31.240	Mehanske konstrukcije za elektronsko opremo	Mechanical structures for electronic equipment

**SIST EN 60191-4:2014**

**en**

**iTeh STANDARD PREVIEW**  
**(standards.iteh.ai)**

[SIST EN 60191-4:2014](#)

<https://standards.iteh.ai/catalog/standards/sist/f11f5eae-f6a8-4954-b8e9-54d38c79aef0/sist-en-60191-4-2014>

EUROPEAN STANDARD  
NORME EUROPÉENNE  
EUROPÄISCHE NORM

**EN 60191-4**

March 2014

ICS 31.080

Supersedes EN 60191-4:1999 + A1:2002 + A2:2002

English version

**Mechanical standardization of semiconductor devices -  
Part 4: Coding system and classification into forms of package outlines  
for semiconductor device packages  
(IEC 60191-4:2013)**

Normalisation mécanique des dispositifs à  
semiconducteurs -  
Partie 4: Système de codification et  
classification en formes des boîtiers pour  
dispositifs à semiconducteurs  
(CEI 60191-4:2013)

Mechanische Normung von  
Halbleiterbauelementen -  
Teil 4: Codierungssystem für Gehäuse  
und Eingruppierung der Gehäuse nach  
der Gehäuseform für  
Halbleiterbauelemente  
(IEC 60191-4:2013)

**iTeh STANDARD PREVIEW  
(standards.iteh.ai)**

[SIST EN 60191-4:2014](https://standards.iteh.ai/catalog/standards/sist/fl1f5eae-f6a8-4954-b8e9-100000000000/EN-60191-4-2014)

<https://standards.iteh.ai/catalog/standards/sist/fl1f5eae-f6a8-4954-b8e9-100000000000/EN-60191-4-2014>

This European Standard was approved by CENELEC on 2013-11-14. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

**CENELEC**

European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**CEN-CENELEC Management Centre: Avenue Marnix 17, B - 1000 Brussels**

## Foreword

The text of document 47D/837/FDIS, future edition 3 of IEC 60191-4, prepared by SC 47D, Semiconductor devices packaging, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-4:2014.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2014-09-21
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2016-11-14

This European Standard supersedes EN 60191-4:1999 and its Amendments A1:2002 and A2:2002.

EN 60191-4:2014 includes the following significant changes with respect to EN 60191-4:1999:

- a) Material code "S" is added to indicate a silicon based package.
- b) Description of "WL" is added to be used for general use.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

**iTeh STANDARD PREVIEW**

**(standards.iteh.ai)**

**Endorsement notice**

The text of the International Standard IEC 60191-4:2013 was approved by CENELEC as a European Standard without any modification.



IEC 60191-4

Edition 3.0 2013-10

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE



**Mechanical standardization of semiconductor devices –  
Part 4: Coding system and classification into forms of package outlines for  
semiconductor device packages**

**Normalisation mécanique des dispositifs à semiconducteurs –  
Partie 4: Système de codification et classification en formes des structures des  
boîtiers pour dispositifs à semiconducteurs**

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

COMMISSION  
ELECTROTECHNIQUE  
INTERNATIONALE

PRICE CODE  
CODE PRIX

T

ICS 31.080

ISBN 978-2-8322-1155-7

**Warning! Make sure that you obtained this publication from an authorized distributor.  
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.**

## CONTENTS

FOREWORD.....	3
1 Scope.....	5
2 Coding system of package outlines for semiconductor devices .....	5
3 Classification into forms of package outlines for semiconductor devices .....	5
4 Coding system for semiconductor-device packages.....	6
4.1 General .....	6
4.2 New descriptive codes .....	6
4.3 Descriptive designators.....	6
4.3.1 General remarks .....	6
4.3.2 Minimum descriptive designator .....	6
4.3.3 Terminal-position prefix.....	8
4.3.4 Package-body-material prefix.....	8
4.3.5 Package-specific feature prefix .....	9
4.3.6 Lead-form and terminal-count suffixes .....	9
4.3.7 Detailed information field .....	11
5 Coding system of package-outline styles .....	12
Annex A (informative) Examples of descriptive coding system application .....	15
Annex B (informative) Derivation and application of the descriptive coding system – Common package names .....	22
<b>(standards.iteh.ai)</b>	
Figure 1 – Descriptive coding for semiconductor device packages .....	7
Figure 2 – Relationship of codes to profile .....	10
Figure A.1 – Typical package styles and descriptive coding system (1 of 4) .....	17
Figure A.2 – Examples of lead forms (or terminal shapes) .....	21
Figure B.1 – Descriptive coding system for common name of semiconductor-device package.....	22
Table 1 – Package-outline-style codes.....	8
Table 2 – Terminal-position prefixes .....	9
Table 3 – Prefixes for predominant package-body material .....	10
Table 4 – Prefixes for package-specific features.....	10
Table 5 – Suffixes for lead form (or terminal shape).....	12
Table A.1 – Descriptive coding system application .....	16
Table B.1 – Basic package code and names.....	23
Table B.2 – Common package name and descriptive code examples .....	24

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –****Part 4: Coding system and classification into forms of package outlines for semiconductor device packages**

## FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user. ([standards.iteh.ai](http://standards.iteh.ai))
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter. (<https://standards.iteh.ai/catalog/standards/sist/f11f5eae-f6a8-4954-b8e9-54d8e70ac9f1/iec-60191-4-2014>)
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-4 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices.

This third edition cancels and replaces the second edition published in 1999, Amendment 1:2001 and Amendment 2:2002. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) Material code "S" is added to indicate a silicon based package.
- b) Description of "WL" is added to be used for general use.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/837/FDIS	47D/848/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, published under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

## iTeh STANDARD PREVIEW

**IMPORTANT – The 'colour inside logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.**

<https://standards.iteh.ai/catalog/standards/sist/f115eae-fba8-4954-b8e9-54d38c79aef0/sist-en-60191-4-2014>



## MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

### Part 4: Coding system and classification into forms of package outlines for semiconductor device packages

#### 1 Scope

This part of IEC 60191 specifies a method for the designation of package outlines and for the classification of forms of package outlines for semiconductor devices and a systematic method for generating universal descriptive designators for semiconductor device packages.

The descriptive designator provides a useful communication tool but has no implied control for assuring package interchangeability.

#### 2 Coding system of package outlines for semiconductor devices

The following coding system will be used in the publications concerning mechanical standardization:

- first: a three-digit serial number (000 to 999);
- second: a single reference letter indicating the form as shown in Table 1;
- third: a two-digit serial number (00 to 99) to indicate a variant of an outline drawing. The use of prefix P to indicate a provisional drawing remains unchanged.

#### Examples

- 101A00
- 050G13
- P 101F01

#### 3 Classification into forms of package outlines for semiconductor devices

The package outline drawings for semiconductor devices are classified into forms according to the following scheme:

- form A: single-ended
- form B: heat-sink-mounted
- form C: stud-mounted
- form D: axial-leaded
- form E: surface-mounted
- form F: single-ended, heat-sink-mounted
- form G: dual and quad in-line
- form H: axial lead-less.

## 4 Coding system for semiconductor-device packages

### 4.1 General

The standard coding system is a method for identifying the physical features of an electronic device package family. The system is predicated upon a minimum two-character designator, which indicates the package outline style. This designator can be extended, through the use of optional, user-selected fields, to provide additional package information such as terminal position and count, terminal form, package shape, and predominant body material.

### 4.2 New descriptive codes

If a new package that does not conform to one of the designated field character codes is being proposed, a new code may be recommended for standardization.

### 4.3 Descriptive designators

#### 4.3.1 General remarks

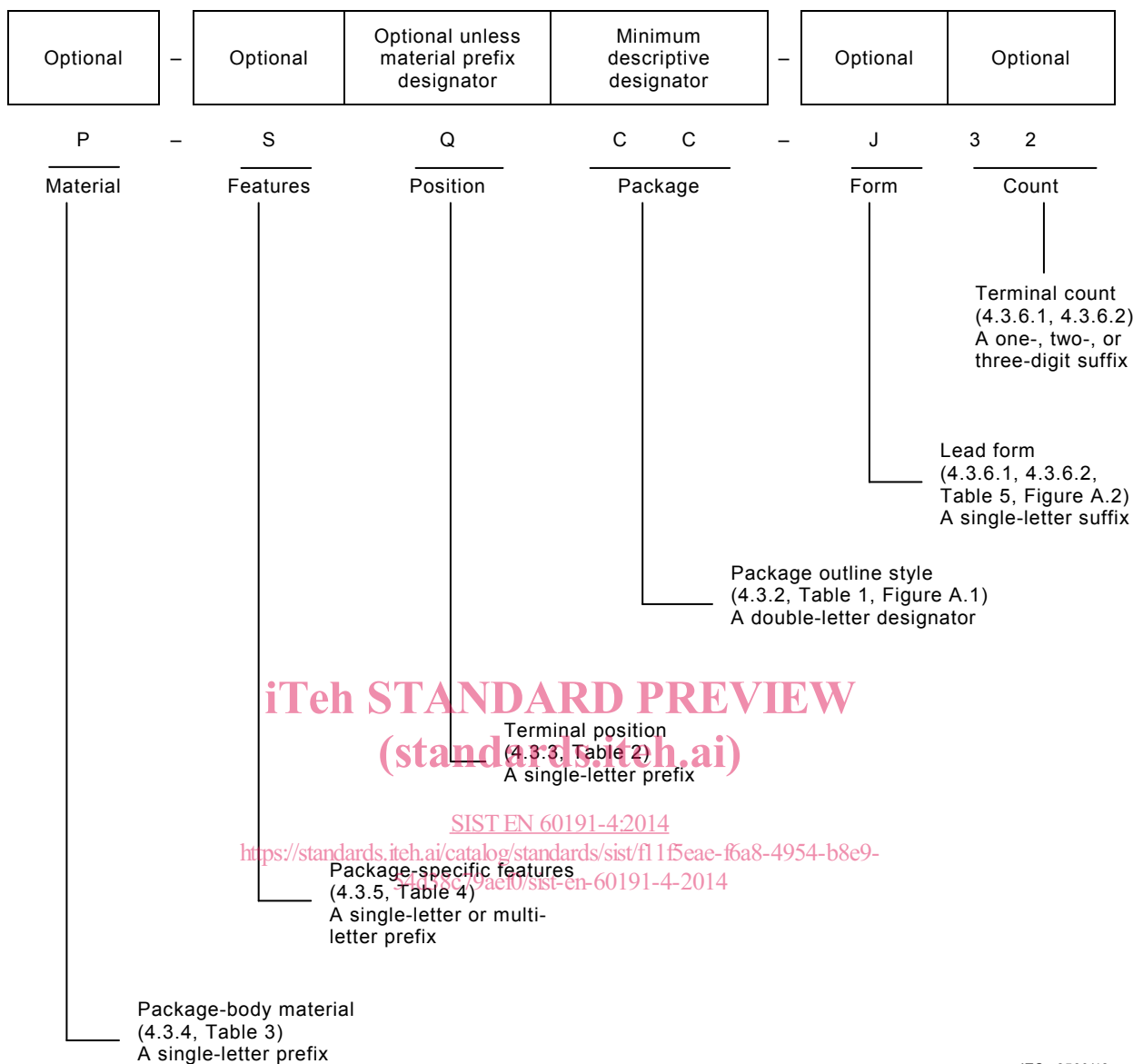
The package outline style code is the only compulsory field within this descriptive designation system. Additional information may be provided using optional prefixes and suffixes described by the system. In general, these fields are independent of one another. Unless otherwise indicated herein, the users of this system may pick and choose which of these fields they wish to implement for their specific application (see Figure 1). The descriptive designator may be extended with additional information, provided this information is separated from the descriptive designator by a slash (/) (see 4.3.7).

NOTE Basic package codes and names are presented in Table B.1.

#### 4.3.2 Minimum descriptive designator

The minimum descriptive designator is a two-letter code that classifies device packages into standard package outline styles. These styles identify general external physical features. Common two-letter descriptive codes or abbreviations are included, such as CC, FP, SO, GA.

Figure A.1 shows two-letter codes for various device package outline styles and depicts examples of each. Table 1 lists the two-letter package-outline-style codes described in Clause 5.



**Figure 1 – Descriptive coding for semiconductor device packages**