Designation: F 533 – 02a

Standard Test Method for Thickness and Thickness Variation of Silicon Wafers[1]

This standard is issued under the fixed designation F 533; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

INTRODUCTION

When this test method was developed in the 1970s, non-contact thickness gages employing manual wafer positioning, which are the basis of this test method, were in routine use. More recently, faster, automated instruments have replaced these manual gages for most common uses in the semiconductor industry. In these automatic systems, microprocessors or microcomputers are used to control wafer positioning, operate the instrument and to analyze the data. See Test Method F 1530.

Despite the fact that this test method is not commonly used in its present form, it embodies all the basic elements of this test method and a simple analysis of data. Thus, it provides useful guidance in the fundamentals and appplication of differential non-contact wafer thickness measurements.

1. Scope

1.1 This test method[2] covers measurement of the thickness of silicon wafers, polished or unpolished, and estimation of the variation in thickness across the wafer.

1.2 This test method is intended primarily for use with wafers that meet the dimension and tolerance requirements of SEMI Specifications M1. However, it can be applied to circular silicon, wafers or substrates of any diameter and thickness that can be handled without breaking.

1.3 This test method is suitable for both contact and contactless gaging equipment. Precision statements have been established for each.

1.4 The values stated in inch-pound units are to be regarded as standard. The values in parentheses are for information only.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 1530 Test Method for Measuring Flatness, Thickness and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning[3]

2.2 *SEMI Standard:*

SEMI M1, Specifications for Polished Monocrystalline Silicon Wafers[4]

2.3 *Federal Standards:*

Fed. Std. No. 209E Controlled Environment Clean Room and Work Station Requirements[5]

Fed. Spec. GGG-G-15C Gage Blocks and Accessories (Inch and Metric), Nov. 6, 1970 [6]

2.4 *ISO Standard*

ISO 14644-1, Cleanrooms and associated controlled environments — Part 1: Classification of airborne particulates[7]

3. Terminology

3.1 *Definitions:*

3.1.1 *back surface—of a semiconductor wafer*, the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Electrical and Optical Measurement.

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[2] DIN 50441/1 is an equivalent method. It is the responsibility of DIN Committee NMP 221, with which Committee F01 maintains close liaison. DIN 50441/1. Determinaton of the Geometric Dimensions of Semiconductor Slices; Measurement of Thickness, available from Beuth Verlag, Gmbh, Burggrafenstrasse 4-10, D-1000 Berlin 30, Federal Republic of Germany.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Semiconductor Equipment and Materials International, 3081 Zanker Road, San Jose, CA 95134 (www.semi.org).

[5] Available from GSA Business Service Centers in Boston, New York, Atlanta, Chicago, Kansas City, Mo., Fort Worth, Denver, San Francisco, Los Angeles, and Seattle.

[6] Available from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402.

[7] ISO Central Secretariat, C. P. 56, CH-1211 Genève 20, Switzerland; available in the U.S. from American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036.

3.1.2 *front surface—of a semiconductor wafer*, the exposed surface upon which active semiconductor devices have been or will be fabricated.

3.1.3 *thickness—of a semiconductor wafer*, the distance through the wafer between corresponding points on the front and back surfaces.

3.1.4 *total thickness variation, TTV—of a semiconductor wafer*, the difference between the maximum and minimum values of the thickness of the wafer.

4. Summary of Test Method

4.1 The thickness of the wafer is measured at its center and at four other sites whose positions are defined with respect to the primary flat or other index mark. Two of the sites fall along a diameter and two along a second diameter, perpendicular to the first.

4.2 The thickness measured at the center of the wafer is generally taken as the nominal thickness of the wafer.

4.3 The maximum difference between any two of the five thickness measurements is taken as the total thickness variation of the wafer.

5. Significance and Use

5.1 Wafer thickness and thickness variations must be controlled to suit the requirements of fixtures and equipment used in microelectronic processing. Estimates of these parameters, based on a representative sample from a given lot of wafers, will aid in determining whether or not wafers from that lot are acceptable for the intended processing steps.

5.2 Wafers that are too thin may break during normal processing operations. Wafers that are too thick may cause mechanical jamming. Wafers with thicknesses outside the desired tolerance may not have appropriate thermal mass or electrical resistance for certain processing steps.

5.3 Excessive thickness variations may cause problems with mechanical handling of the wafers during processing. In addition, such variations may cause deviations from surface flatness that adversely affect photolithographic processes. The effect of thickness variations on photolithographic processes depends on the line width and registration requirements of individual circuit designs, as well as on the specific optical and mechanical design of the photolithographic processing equipment being used.

5.4 This test method is intended for use for materials acceptance and process control purposes. This test method may be applied at any point during the processing of unpolished wafers into polished wafers or substrates.

6. Inferferences

6.1 Since the determination of total thickness variation by this test method is based on measurements of wafer thickness at only five sites, irregular geometrical variations in other parts of the wafer will not be detected.

6.2 Local changes in thickness at any site may result in erroneous readings. Such local changes in thickness may be caused by surface defects such as chips, contaminants, mounds, pits, saw steps, waves, and so forth.

7. Apparatus

7.1 *Thickness Gage*, suitable for measuring the thickness of semiconductor wafers over the anticipated range. The least count of the instrument shall be no larger than 0.0001 in., or 2 µm. The contact area for contact-type gages shall not exceed 0.003 in.^{2} (2 mm^2). For contactless gages, the probed area shall not exceed 0.2 in.^{2} (129 mm^2).

NOTE 1—Thickness ranges for standard silicon wafers are given in SEMI Specifications M1. A thickness gage covering the range from 0.005 to 0.050 in. (0.13 to 1.3 mm) should be adequate for most wafers. A wafer with thickness outside this range may be mechanically accommodated by the gage; an appropriate offset is then applied to the value indicated by the gage.

7.2 *Fixture*, to support the wafer during thickness measurements. The fixture shall include provision for rotating the wafer about its center in the wafer plane and sufficient markings to facilitate positioning of the wafer so that thickness measurements can be made within 0.08 in. (2 mm) of each specified measurement site (see Fig. 1).

7.3 *Clean Facility*—A controlled-environment work station satisfying the Class 7 requirements of ISO 14644-1.

NOTE 2—ISO Class 7 is about the same as Class 10 000 as defined in Fed Std 209E.

7.4 *Scribe*—A scribe or other means for producing an index mark on the wafer, if required.

7.5 *Thickness Calibration Standards*—A set of thickness standards, traceable to the National Bureau of Standards, whose nominal thickness values range from 0.005 to 0.050 in. (0.13 to 1.27 mm) in steps of 0.005 ± 0.001 in. (0.13 ± 0.025 mm).

7.5.1 Standard thickness values shall be known to within 10 µin. (0.25 µm).

7.5.2 For contactless gages, the calibration standards shall have an area of at least 0.25 in.^{2} (1.6 cm^2) with a minimum side length of 0.5 in. (13 mm). The thickness variation must be less than 0.0001 in., or 2 µm, as determined for any two points 1 in. (25 mm) apart. See Note 6.

7.5.3 For contact gages, normally available standards of 0.36 by 1.12 in. (9.1 by 28.4 mm) shall be acceptable.

NOTE 3—Further details are available in Fed. Spec. GGG-G-15C.

8. Sampling

8.1 This test method is intended to be used on a sampling basis. Procedures for selecting the sample from each lot of wafers to be tested shall be agreed upon between the parties to the test, as shall the definition of what constitutes a lot.

9. Test Specimen

9.1 If the specimen wafer does not contain reference flats, such as those specified in SEMI Specifications M1, use the scribe to place an index mark at a point near the periphery of the back surface of the wafer.

9.2 Ensure that the specimen has an identifiable surface to enable interlaboratory location of measurement sites.

9.2.1 If the front and back specimen surfaces are different in appearance, specify the front surface.