SIST

SLOVENSKI STANDARD
SIST EN 60191-6-22:2013

01-junij-2013

Standardizacija mehanskih lastnosti polprevodniških elementov - 6-22. del: Splošna pravila za pripravo tehničnih risb okrovov polprevodniških elementov za površinsko montažo - Vodilo za oblikovanje okrovov polprevodnikov s finim rastrom mreže krogličastih priključkov na siliciju (S-FBGA) in finim rastrom mreže priključkov v ravnini na siliciju (S-FLGA)

Mechanical Standardization Of Semiconductor Devices - Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)

iTeh STANDARD PREVIEW
(standards.iteh.ai)

/

SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

/

Ta slovenski standard je istoveten z: EN 60191-6-22:2013

ICS:

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

SIST EN 60191-6-22:2013 **en**

2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

SIST EN 60191-6-22:2013

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

SIST EN 60191-6-22:2013

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60191-6-22

March 2013

ICS 31.080.01

English version

Mechanical standardization of semiconductor devices - Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)

(IEC 60191-6-22:2012)

Normalisation mécanique des dispositifs à semiconducteurs -
Partie 6-22: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface -
Guide de conception pour les boîtiers matriciels à billes et à pas fins en silicium et boîtiers matriciels à zone de contact plate et à pas fins en silicium
(S-FBGA et S-FLGA)
(CEI 60191-6-22:2012)

Mechanische Normung von Halbleiterbauelementen -
Teil 6-22: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen -
Konstruktionsleitfaden für Halbleitergehäuse Si-Feinraster-Ball-Grid-Array und Si-Feinraster-Land-Grid-Array
(S-FBGA und S-FLGA)
(IEC 60191-6-22:2012)

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

This European Standard was approved by CENELEC on 2013-01-15. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

© 2013 CENELEC - All rights of exploitation in any form and by any means reserved worldwide for CENELEC members.

Ref. No. EN 60191-6-22:2013 E

SIST EN 60191-6-22:2013

Foreword

The text of document 47D/812/CDV, future edition 1 of IEC 60191-6-22, prepared by SC 47D, "Semiconductor packaging", of IEC TC 47, "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 60191-6-22:2013.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2013-10-15
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2016-01-15

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

Endorsement notice

The text of the International Standard IEC 60191-6-22:2012 was approved by CENELEC as a European Standard without any modification.

SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/...
8fb2a0246451/sist-en-60191-6-22-2013

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60191-6	NOTE	Harmonized as EN 60191-6.
IEC 60191-6-5	NOTE	Harmonized as EN 60191-6-5.
IEC 60191-6-12	NOTE	Harmonized as EN 60191-6-12.

SIST EN 60191-6-22:2013

IEC 60191-6-22

Edition 1.0 2012-12

INTERNATIONAL STANDARD

NORME INTERNATIONALE

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

Mechanical standardization of semiconductor devices – Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)

Normalisation mécanique des dispositifs à semiconducteurs – Partie 6-22: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface – Guide de conception pour les boîtiers matriciels à billes et à pas fins en silicium et boîtiers matriciels à zone de contact plate et à pas fins en silicium (S-FBGA et S-FLGA)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX

ICS 31.080.01

ISBN 978-2-83220-526-6

Warning! Make sure that you obtained this publication from an authorized distributor.
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

® Registered trademark of the International Electrotechnical Commission
Marque déposée de la Commission Electrotechnique Internationale

SIST EN 60191-6-22:2013

CONTENTS

FOREWORD ... 3
1 Scope ... 5
2 Normative references ... 5
3 Terms and definitions ... 5
4 Terminal position numbering ... 5
5 Code of package nominal dimensions ... 5
6 Symbols and drawings ... 6
7 Dimensions ... 9
7.1 Group 1 ... 9
7.2 Group 2 ... 11
8 Combination list of D, E, M_D, and M_E ... 12
Bibliography ... 17

Figure 1 – S-FBGA outline ... 6
Figure 2 – S-FLGA outline ... 7
Figure 3 – Mechanical gauge drawing[e)] ... 8
Figure 4 – Array of terminal-existence areas[f)] ... 8

Table 1 – Dimensions and tolerances in Group 1 ... 9
Table 2 – Dimensions and tolerances of Group 2 ... 11
Table 3 – $\boxed{e}$ = 0,80 mm pitch S-FBGA and S-FLGA ... 12
Table 4 – $\boxed{e}$ = 0,65 mm pitch S-FBGA and S-FLGA ... 12
Table 5 – $\boxed{e}$ = 0,50 mm pitch S-FBGA and S-FLGA ... 13
Table 6 – $\boxed{e}$ = 0,40 mm pitch S-FBGA and S-FLGA ... 14
Table 7 – $\boxed{e}$ = 0,30 mm pitch S-FBGA and S-FLGA ... 15
Table 8 – $\boxed{e}$ = 0,25 mm pitch S-FLGA ... 16

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-
9f63e624f4f3/sist-en-60191-6-22-2013

SIST EN 60191-6-22:2013

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854e385-ee5e-4b7d-a637-
0b82a2464341/sist-en-60191-6-22-2013

International Standard IEC 60191-6-22 has been prepared by subcommittee 47D: Semiconductor packaging, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

CDV	Report on voting
47D/812/CDV	47D/820/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

SIST EN 60191-6-22:2013

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

SIST EN 60191-6-22:2013

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)

1 Scope

This part of IEC 60191 provides the outline drawings and dimensions common to silicon-based package structures and materials of ball grid array packages (BGA) and land grid array packages (LGA).

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

Void

3 Terms and definitions

SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-
8b2b0a4bf057/sist-en-60191-6-22-2013

For the purpose of this document, the following terms and definitions apply.

3.1
S-FBGA
FBGA composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer balls on the dielectric layer(s), and outer balls with heights more than 0,1 mm

3.2
S-FLGA
FLGA composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer lands on the dielectric layer(s), and outer lands with heights of 0,1 mm or less

4 Terminal position numbering

When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C…, AA, AB, etc., whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, e.g., A1, B1.

The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

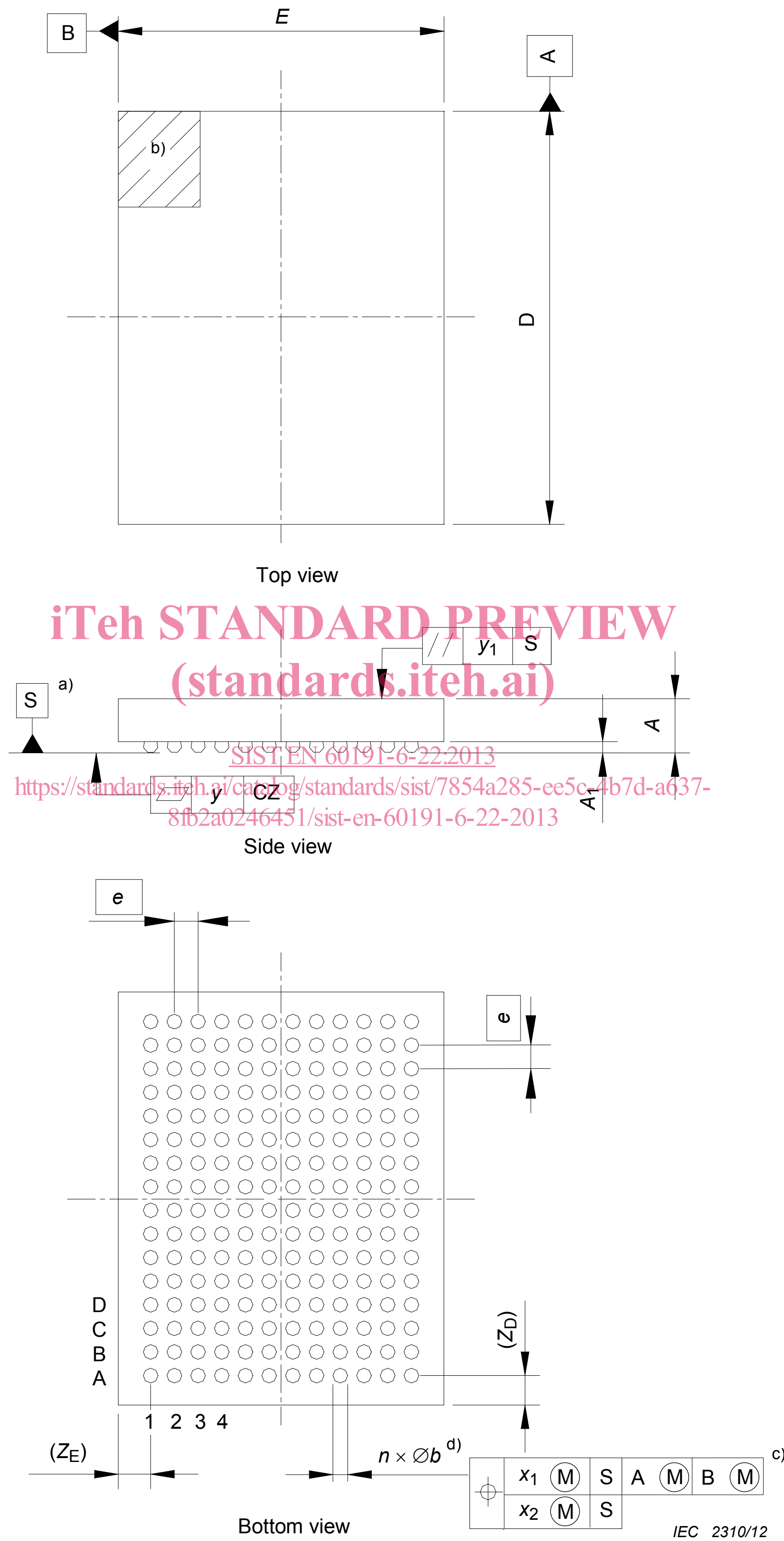
5 Code of package nominal dimensions

A code of package nominal dimensions is defined as the combination of package width *E* and length *D* which are shown in the second decimal place in millimeter.

SIST EN 60191-6-22:2013

6 Symbols and drawings

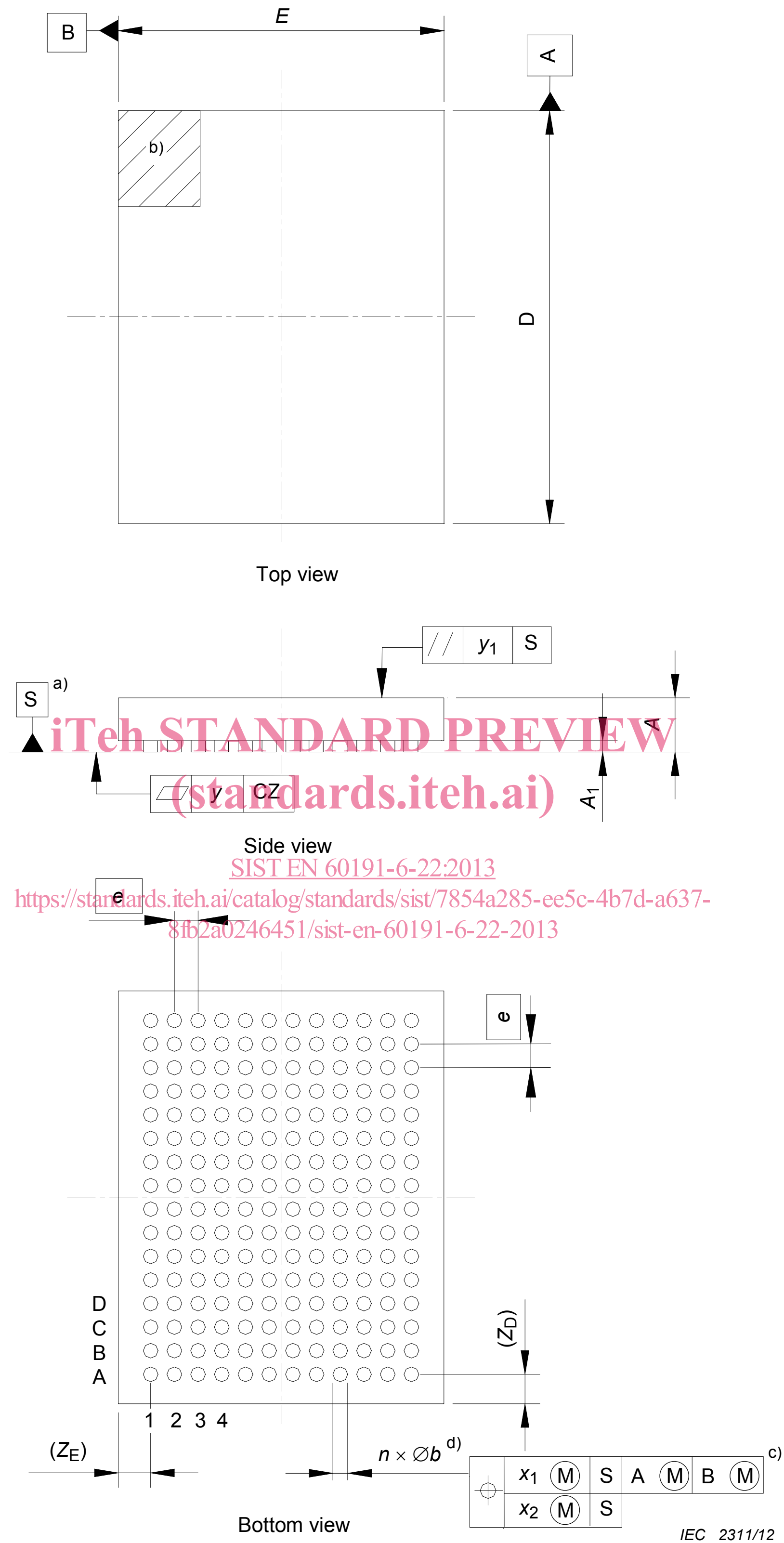
Symbols and drawings are shown in Figures 1, 2, 3 and 4.



iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

Figure 1 – S-FBGA outline

SIST EN 60191-6-22:2013



iTeh STANDARD PREVIEW
(standards.iteh.ai)
SIST EN 60191-6-22:2013
https://standards.iteh.ai/catalog/standards/sist/7854a285-ee5c-4b7d-a637-8fb2a0246451/sist-en-60191-6-22-2013

Figure 2 – S-FLGA outline