
Programirljivi kontrolniki - 9. del: Enožični digitalni komunikacijski vmesnik za male senzorje in dajalnike (SDCI) (IEC 61131-9:2013)

Programmable controllers - Part 9: Single-drop digital communication interface for small sensors and actuators (SDCI) (IEC 61131-9:2013)

Speicherprogrammierbare Steuerungen - Teil 9: Leitlinien für die Anwendung und Implementierung von Programmiersprachen für Speicherprogrammierbare Steuerungen (IEC 61131-9:2013)

(standards.iteh.ai)

Automates programmables - Partie 9: Interface de communication numérique point à point pour les petits capteurs et actionneurs (SDCI) (CEI 61131-9:2013)

Ta slovenski standard je istoveten z: EN 61131-9:2013

ICS:

25.040.40	Merjenje in krmiljenje industrijskih postopkov	Industrial process measurement and control
35.240.50	Uporabniške rešitve IT v industriji	IT applications in industry

SIST EN 61131-9:2014**en**

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 61131-9:2014](#)

<https://standards.iteh.ai/catalog/standards/sist/1a45c6d9-d4f6-4182-8d1f-ba70a1e763fe/sist-en-61131-9-2014>

EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 61131-9

December 2013

ICS 25.040.40; 35.240.50

English version

**Programmable controllers -
Part 9: Single-drop digital communication interface for small sensors and
actuators (SDCI)
(IEC 61131-9:2013)**

Automates programmables -
Partie 9: Interface de communication
numérique point à point pour petits
capteurs et actionneurs (SDCI)
(CEI 61131-9:2013)

Speicherprogrammierbare Steuerungen -
Teil 9: Schnittstelle für die Kommunikation
mit kleinen Sensoren und Aktoren über
eine Punkt-zu-Punkt-Verbindung
(IEC 61131-9:2013)

iTeh STANDARD PREVIEW
(standards.iteh.ai)

This European Standard was approved by CENELEC on 2013-10-16. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B - 1000 Brussels

Foreword

The text of document 65B/874/FDIS, future edition 1 of IEC 61131-9, prepared by SC 65B, "Measurement and control devices", of IEC/TC 65, "Industrial-process measurement, control and automation" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 61131-9:2013.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2014-07-16
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2016-10-16

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 61131-9:2013 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60870-5-1:1990	NOTE	Harmonised as EN 60870-5-1:1993 (not modified).
IEC 61158-2	NOTE	Harmonised as EN 61158-2 (not modified).
IEC/TR 62453-61	NOTE	Harmonised as CLC/TR 62453-61 (not modified).
ISOIEC 7498-1	NOTE	Harmonised as EN ISOIEC 7498-1 (not modified).

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60947-5-2	-	Low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - Proximity switches	EN 60947-5-2	-
IEC 61000-4-2	-	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test	EN 61000-4-2	-
IEC 61000-4-3	-	Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated radio-frequency electromagnetic field immunity test	EN 61000-4-3	-
IEC 61000-4-4	-	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	-
IEC 61000-4-5	-	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test	FprEN 61000-4-5	-
IEC 61000-4-6	-	Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields	FprEN 61000-4-6	-
IEC 61000-4-11	-	Electromagnetic compatibility (EMC) - Part 4-11: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests	EN 61000-4-11	-
IEC 61000-6-2	-	Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity for industrial environments	EN 61000-6-2 + corr. September	-
IEC 61000-6-4	-	Electromagnetic compatibility (EMC) - Part 6-4: Generic standards - Emission standard for industrial environments	EN 61000-6-4	-
IEC 61076-2-101	-	Connectors for electronic equipment - Product requirements - Part 2-101: Circular connectors - Detail specification for M12 connectors with screw-locking	EN 61076-2-101	-
IEC 61131-1	-	Programmable controllers - Part 1: General information	EN 61131-1	-

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 61131-2	-	Programmable controllers - Part 2: Equipment requirements and tests	EN 61131-2 ¹⁾	-
IEC/TR 62390	-	Common automation device - Profile guideline	-	-
ISO/IEC 646	1991	Information technology - ISO 7-bit coded character set for information interchange	-	-
ISO/IEC 2022	-	Information technology - Character code structure and extension techniques	-	-
ISO/IEC 10646	-	Information technology - Universal Coded Character Set (UCS)	-	-
ISO/IEC 10731	-	Information technology - Open Systems Interconnection - Basic reference model - Conventions for the definition of OSI services	-	-
ISO 1177	-	Information processing - Character structure for start/stop and synchronous character-oriented transmission	-	-
IEEE 754	2008	Binary floating-point arithmetic	-	-

iTeh STANDARD PREVIEW (standards.iteh.ai)

[SIST EN 61131-9:2014](https://standards.iteh.ai/catalog/standards/sist/1a45c6d9-d4f6-4182-8d1f-ba70a1e763fe/sist-en-61131-9-2014)

<https://standards.iteh.ai/catalog/standards/sist/1a45c6d9-d4f6-4182-8d1f-ba70a1e763fe/sist-en-61131-9-2014>

¹⁾ EN 61131-2 is superseded by EN 61010-2-201:2013, which is based on IEC 61010-2-201:2013.



IEC 61131-9

Edition 1.0 2013-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE



Programmable controllers –
Part 9: Single-drop digital communication interface for small sensors and actuators (SDCI)

Automates programmables –
Partie 9: Interface de communication numérique point à point pour petits capteurs et actionneurs (SDCI)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX

XH

ICS 25.040.40; 35.240.50

ISBN 978-2-8322-1076-5

Warning! Make sure that you obtained this publication from an authorized distributor.
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

CONTENTS

FOREWORD.....	14
INTRODUCTION.....	16
1 Scope.....	18
2 Normative references	18
3 Terms, definitions, symbols, abbreviated terms and conventions	19
3.1 Terms and definitions	19
3.2 Symbols and abbreviated terms.....	23
3.3 Conventions	25
3.3.1 General	25
3.3.2 Service parameters	25
3.3.3 Service procedures.....	26
3.3.4 Service attributes	26
3.3.5 Figures	26
3.3.6 Transmission octet order	26
3.3.7 Behavioral descriptions	27
4 Overview of SDCI (IO-Link™).....	27
4.1 Purpose of technology.....	27
4.2 Positioning within the automation hierarchy	28
4.3 Wiring, connectors and power	29
4.4 Communication features of SDCI.....	29
4.5 Role of a Master.....	31
4.6 SDCI configuration	32
4.7 Mapping to fieldbuses	32
4.8 Standard structure.....	32
5 Physical Layer (PL)	33
5.1 General	33
5.1.1 Basics	33
5.1.2 Topology	33
5.2 Physical layer services	34
5.2.1 Overview	34
5.2.2 PL services.....	35
5.3 Transmitter/Receiver	37
5.3.1 Description method.....	37
5.3.2 Electrical requirements	37
5.3.3 Timing requirements	41
5.4 Power supply.....	44
5.4.1 Power supply options	44
5.4.2 Power-on requirements.....	45
5.5 Medium	45
5.5.1 Connectors	45
5.5.2 Cable.....	47
6 Standard Input and Output (SIO)	48
7 Data link layer (DL)	48
7.1 General	48
7.2 Data link layer services	50
7.2.1 DL-B services	50

7.2.2	DL-A services	61
7.3	Data link layer protocol.....	66
7.3.1	Overview	66
7.3.2	DL-mode handler	67
7.3.3	Message handler	75
7.3.4	Process Data handler	82
7.3.5	On-request Data handler	85
7.3.6	ISDU handler.....	88
7.3.7	Command handler	92
7.3.8	Event handler	95
8	Application layer (AL)	98
8.1	General.....	98
8.2	Application layer services.....	99
8.2.1	AL services within Master and Device.....	99
8.2.2	AL Services	100
8.3	Application layer protocol	108
8.3.1	Overview	108
8.3.2	On-request Data transfer	108
8.3.3	Event processing	114
8.3.4	Process Data cycles	117
9	System management (SM)	118
9.1	General.....	118
9.2	System management of the Master	118
9.2.1	Overview	118
9.2.2	SM Master services	120
9.2.3	SM Master protocol	125
9.3	System management of the Device	133
9.3.1	Overview	133
9.3.2	SM Device services	135
9.3.3	SM Device protocol	141
10	Device.....	148
10.1	Overview	148
10.2	Process Data Exchange (PDE).....	149
10.3	Parameter Manager (PM)	149
10.3.1	General	149
10.3.2	Parameter manager state machine	149
10.3.3	Dynamic parameter	151
10.3.4	Single parameter	152
10.3.5	Block parameter	153
10.3.6	Concurrent parameterization access.....	155
10.3.7	Command handling.....	155
10.4	Data Storage (DS).....	155
10.4.1	General	155
10.4.2	Data Storage state machine	155
10.4.3	DS configuration.....	157
10.4.4	DS memory space	157
10.4.5	DS Index_List.....	158
10.4.6	DS parameter availability.....	158
10.4.7	DS without ISDU.....	158

10.4.8	DS parameter change indication	158
10.5	Event Dispatcher (ED).....	158
10.6	Device features	158
10.6.1	General	158
10.6.2	Device backward compatibility	159
10.6.3	Protocol revision compatibility	159
10.6.4	Factory settings	159
10.6.5	Application reset.....	159
10.6.6	Device reset	159
10.6.7	Visual SDCI indication	159
10.6.8	Parameter access locking.....	160
10.6.9	Data Storage locking	160
10.6.10	Device parameter locking	160
10.6.11	Device user interface locking	160
10.6.12	Offset time.....	160
10.6.13	Data Storage concept	161
10.6.14	Block Parameter	161
10.7	Device design rules and constraints	161
10.7.1	General	161
10.7.2	Process Data.....	161
10.7.3	Communication loss	161
10.7.4	Direct Parameter.....	161
10.7.5	ISDU communication channel	162
10.7.6	DeviceID rules related to Device variants	162
10.7.7	Protocol constants	162
10.8	IO Device description (IODD).....	163
10.9	Device diagnosis	163
10.9.1	Concepts	163
10.9.2	Events	164
10.9.3	Visual indicators	165
10.10	Device connectivity	166
11	Master	166
11.1	Overview	166
11.1.1	Generic model for the system integration of a Master	166
11.1.2	Structure and services of a Master	166
11.2	Configuration Manager (CM)	169
11.2.1	General	169
11.2.2	Configuration parameter	171
11.2.3	State machine of the Configuration Manager	173
11.3	Data Storage (DS).....	175
11.3.1	Overview	175
11.3.2	DS data object.....	175
11.3.3	DS state machine	175
11.3.4	Parameter selection for Data Storage	181
11.4	On-Request Data exchange (ODE).....	181
11.5	Diagnosis Unit (DU).....	182
11.6	PD Exchange (PDE).....	183
11.6.1	General	183
11.6.2	Process Data mapping.....	183

11.6.3 Process Data invalid/valid qualifier status	184
11.7 Port and Device configuration tool (PDCT)	185
11.7.1 General	185
11.7.2 Basic layout examples	185
11.8 Gateway application	186
11.8.1 General	186
11.8.2 Changing Device configuration including Data Storage	186
11.8.3 Parameter server and recipe control	186
11.8.4 Anonymous parameters	186
11.8.5 Virtual port mode DIwithSDCI	187
Annex A (normative) Codings, timing constraints, and errors	190
Annex B (normative) Parameter and commands	211
Annex C (normative) ErrorTypes (ISDU errors)	228
Annex D (normative) EventCodes (diagnosis information)	233
Annex E (normative) Data types	236
Annex F (normative) Structure of the Data Storage data object	247
Annex G (normative) Master and Device conformity	248
Annex H (informative) Residual error probabilities	254
Annex I (informative) Example sequence of an ISDU transmission	256
Annex J (informative) Recommended methods for detecting parameter changes	258
Bibliography	259
Figure 1 – Example of a confirmed service	26
Figure 2 – Memory storage and transmission order for WORD based data types	27
Figure 3 – SDCI compatibility with IEC 61131-2	27
Figure 4 – Domain of the SDCI technology within the automation hierarchy	28
Figure 5 – Generic Device model for SDCI (Master's view)	29
Figure 6 – Relationship between nature of data and transmission types	30
Figure 7 – Object transfer at the application layer level (AL)	31
Figure 8 – Logical structure of Master and Device	32
Figure 9 – Three wire connection system	33
Figure 10 – Topology of SDCI	34
Figure 11 – Physical layer (Master)	34
Figure 12 – Physical layer (Device)	35
Figure 13 – Line driver reference schematics	37
Figure 14 – Receiver reference schematics	37
Figure 15 – Reference schematics for SDCI 3-wire connection system	38
Figure 16 – Voltage level definitions	38
Figure 17 – Switching thresholds	39
Figure 18 – Format of an SDCI UART frame	41
Figure 19 – Eye diagram for the 'H' and 'L' detection	42
Figure 20 – Eye diagram for the correct detection of a UART frame	42
Figure 21 – Wake-up request	44
Figure 22 – Power-on timing for Power1	45

Figure 23 – Pin layout front view	46
Figure 24 – Class A and B port definitions	47
Figure 25 – Reference schematic for effective line capacitance and loop resistance	47
Figure 26 – Structure and services of the data link layer (Master)	49
Figure 27 – Structure and services of the data link layer (Device)	49
Figure 28 – State machines of the data link layer	67
Figure 29 – Example of an attempt to establish communication	67
Figure 30 – Failed attempt to establish communication	68
Figure 31 – Retry strategy to establish communication	68
Figure 32 – Fallback procedure	69
Figure 33 – State machine of the Master DL-mode handler	70
Figure 34 – Submachine 1 to establish communication	71
Figure 35 – State machine of the Device DL-mode handler	73
Figure 36 – SDCI message sequences	75
Figure 37 – Overview of M-sequence types	76
Figure 38 – State machine of the Master message handler	77
Figure 39 – Submachine "Response 3" of the message handler	78
Figure 40 – Submachine "Response 8" of the message handler	78
Figure 41 – Submachine "Response 15" of the message handler	78
Figure 42 – State machine of the Device message handler	81
Figure 43 – Interleave mode for the segmented transmission of Process Data	83
Figure 44 – State machine of the Master Process Data handler	83
Figure 45 – State machine of the Device Process Data handler	85
Figure 46 – State machine of the Master On-request Data handler	86
Figure 47 – State machine of the Device On-request Data handler	87
Figure 48 – Structure of the ISDU	88
Figure 49 – State machine of the Master ISDU handler	90
Figure 50 – State machine of the Device ISDU handler	91
Figure 51 – State machine of the Master command handler	93
Figure 52 – State machine of the Device command handler	94
Figure 53 – State machine of the Master Event handler	96
Figure 54 – State machine of the Device Event handler	97
Figure 55 – Structure and services of the application layer (Master)	98
Figure 56 – Structure and services of the application layer (Device)	99
Figure 57 – OD state machine of the Master AL	109
Figure 58 – OD state machine of the Device AL	110
Figure 59 – Sequence diagram for the transmission of On-request Data	112
Figure 60 – Sequence diagram for On-request Data in case of errors	113
Figure 61 – Sequence diagram for On-request Data in case of timeout	113
Figure 62 – Event state machine of the Master AL	114
Figure 63 – Event state machine of the Device AL	115
Figure 64 – Single Event scheduling	116
Figure 65 – Sequence diagram for output Process Data	117

Figure 66 – Sequence diagram for input Process Data.....	118
Figure 67 – Structure and services of the Master system management	119
Figure 68 – Sequence chart of the use case "port x setup"	120
Figure 69 – Main state machine of the Master system management.....	126
Figure 70 – SM Master submachine CheckCompatibility_1	128
Figure 71 – Activity for state "CheckVxy"	130
Figure 72 – Activity for state "CheckCompV10".....	130
Figure 73 – Activity for state "CheckComp".....	131
Figure 74 – Activity (write parameter) in state "RestartDevice".....	131
Figure 75 – SM Master submachine CheckSerNum_3.....	132
Figure 76 – Activity (check SerialNumber) for state CheckSerNum_3.....	133
Figure 77 – Structure and services of the system management (Device).....	134
Figure 78 – Sequence chart of the use case "INACTIVE – SIO – SDCI – SIO"	135
Figure 79 – State machine of the Device system management.....	142
Figure 80 – Sequence chart of a regular Device startup.....	145
Figure 81 – Sequence chart of a Device startup in compatibility mode	146
Figure 82 – Sequence chart of a Device startup when compatibility fails	147
Figure 83 – Structure and services of a Device	148
Figure 84 – The Parameter Manager (PM) state machine	150
Figure 85 – Positive and negative parameter checking result.....	152
Figure 86 – Positive block parameter download with Data Storage request.....	153
Figure 87 – Negative block parameter download.....	154
Figure 88 – The Data Storage (DS) state machine.....	156
Figure 89 – Data Storage request message sequence	157
Figure 90 – Cycle timing	160
Figure 91 – Event flow in case of successive errors	165
Figure 92 – Device LED indicator timing	165
Figure 93 – Generic relationship of SDCI technology and fieldbus technology	166
Figure 94 – Structure and services of a Master	168
Figure 95 – Relationship of the common Master applications	168
Figure 96 – Sequence diagram of configuration manager actions.....	170
Figure 97 – Ports in MessageSync mode	171
Figure 98 – State machine of the Configuration Manager	173
Figure 99 – Main state machine of the Data Storage mechanism	175
Figure 100 – Submachine "UpDownload_2" of the Data Storage mechanism	176
Figure 101 – Data Storage submachine "Upload_7"	177
Figure 102 – Data Storage upload sequence diagram	177
Figure 103 – Data Storage submachine "Download_10".....	178
Figure 104 – Data Storage download sequence diagram.....	178
Figure 105 – State machine of the On-request Data Exchange	181
Figure 106 – System overview of SDCI diagnosis information propagation via Events	183
Figure 107 – Process Data mapping from ports to the gateway data stream.....	184
Figure 108 – Propagation of PD qualifier status between Master and Device	184

Figure 109 – Example 1 of a PDCT display layout.....	185
Figure 110 – Example 2 of a PDCT display layout.....	186
Figure 111 – Alternative Device configuration	187
Figure 112 – Virtual port mode "DIwithSDCI"	188
Figure A.1 – M-sequence control	190
Figure A.2 – Checksum/M-sequence type octet	191
Figure A.3 – Checksum/status octet.....	192
Figure A.4 – Principle of the checksum calculation and compression	193
Figure A.5 – M-sequence TYPE_0	194
Figure A.6 – M-sequence TYPE_1_1	194
Figure A.7 – M-sequence TYPE_1_2	195
Figure A.8 – M-sequence TYPE_1_V	195
Figure A.9 – M-sequence TYPE_2_1	196
Figure A.10 – M-sequence TYPE_2_2	196
Figure A.11 – M-sequence TYPE_2_3	196
Figure A.12 – M-sequence TYPE_2_4	197
Figure A.13 – M-sequence TYPE_2_5	197
Figure A.14 – M-sequence TYPE_2_6	197
Figure A.15 – M-sequence TYPE_2_V	198
Figure A.16 – M-sequence timing.....	201
Figure A.17 – I-Service octet	203
Figure A.18 – Check of ISDU integrity via CHKPDU.....	205
Figure A.19 – Examples of request formats for ISDUs.....	206
Figure A.20 – Examples of response ISDUs.....	206
Figure A.21 – Examples of read and write request ISDUs	207
Figure A.22 – Structure of StatusCode type 1	208
Figure A.23 – Structure of StatusCode type 2	208
Figure A.24 – Indication of activated Events	209
Figure A.25 – Structure of the EventQualifier	209
Figure B.1 – Classification and mapping of Direct Parameters	211
Figure B.2 – MinCycleTime.....	213
Figure B.3 – M-sequence Capability	214
Figure B.4 – RevisionID	215
Figure B.5 – ProcessDataIn	215
Figure B.6 – Index space for ISDU data objects	217
Figure B.7 – Structure of the Offset Time.....	226
Figure E.1 – Coding examples of UIntegerT.....	237
Figure E.2 – Coding examples of IntegerT	239
Figure E.3 – Singular access of StringT	240
Figure E.4 – Coding example of OctetStringT	241
Figure E.5 – Definition of TimeT	241
Figure E.6 – Example of an ArrayT data structure.....	243
Figure E.7 – Example 2 of a RecordT structure.....	245

Figure E.8 – Example 3 of a RecordT structure	245
Figure E.9 – Write requests for example 3	246
Figure G.1 – Test setup for electrostatic discharge (Master)	250
Figure G.2 – Test setup for RF electromagnetic field (Master)	250
Figure G.3 – Test setup for fast transients (Master)	251
Figure G.4 – Test setup for RF common mode (Master)	251
Figure G.5 – Test setup for electrostatic discharges (Device)	252
Figure G.6 – Test setup for RF electromagnetic field (Device)	252
Figure G.7 – Test setup for fast transients (Device)	252
Figure G.8 – Test setup for RF common mode (Device)	253
Figure H.1 – Residual error probability for the SDCl data integrity mechanism	254
Figure I.1 – Example for ISDU transmissions (1 of 2)	256
Table 1 – Service assignments of Master and Device	35
Table 2 – PL_SetMode	35
Table 3 – PL_WakeUp	36
Table 4 – PL_Transfer	36
Table 5 – Electric characteristics of a receiver	39
Table 6 – Electric characteristics of a Master port	39
Table 7 – Electric characteristics of a Device	40
Table 8 – Dynamic characteristics of the transmission	43
Table 9 – Wake-up request characteristics	44
Table 10 – Power-on timing	45
Table 11 – Pin assignments	46
Table 12 – Cable characteristics	47
Table 13 – Cable conductor assignments	48
Table 14 – Service assignments within Master and Device	50
Table 15 – DL_ReadParam	51
Table 16 – DL_WriteParam	51
Table 17 – DL_Read	52
Table 18 – DL_Write	53
Table 19 – DL_ISDUTransport	54
Table 20 – DL_ISDUAbort	55
Table 21 – DL_PDOutputUpdate	55
Table 22 – DL_PDOutputTransport	56
Table 23 – DL_PDInputUpdate	57
Table 24 – DL_PDInputTransport	57
Table 25 – DL_PDCycle	58
Table 26 – DL_SetMode	58
Table 27 – DL_Mode	59
Table 28 – DL_Event	60
Table 29 – DL_EventConf	60
Table 30 – DL_EventTrigger	61