INTERNATIONAL STANDARD

ISO/IEC 10536-3

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Identification cards — Contactless integrated circuit(s) cards —

Part 3:
Electronic signals and reset procedures

Cartes d'identification — Cartes à circuit(s) intégré(s) sans contact —

Partie 3: Signaux électroniques et procédures de réinitialisation

Reference number
ISO/IEC 10536-3:1996(E)

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organizations to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote.

International Standard ISO/IEC 10536-3 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Identification cards and related devices*.

ISO/IEC 10536 consists of the following parts, under the general title *Identification cards - Contactless integrated circuit(s) cards*:

- *Part 1: Physical characteristics*

- *Part 2: Dimensions and locations of coupling areas*

- *Part 3: Electronic signals and reset procedures*

Annexes A to D form an integral part of this part of ISO/IEC 10536.

Introduction

ISO/IEC 10536 is one of a series of International Standards describing the parameters for identification cards as defined in ISO 7810 and the use of such cards for international interchange.

This part of ISO/IEC 10536 describes the electronic characteristics of the contactless interface between a contactless integrated circuit(s) card and a card-coupling device. The interfaces include power and bi-directional communications.

Identification cards — Contactless integrated circuit(s) cards —

Part 3:
Electronic signals and reset procedures

1 Scope

This part of ISO/IEC 10536 specifies the nature and characteristics of the fields to be provided for power and bi-directional communications between card coupling devices (CCDs) and contactless integrated circuit(s) cards (CICCs) of the ID-1 card type in slot or surface operation.

This part of ISO/IEC 10536 does not specify the means of generating coupling fields, nor the means of compliance with electromagnetic radiation regulations.

This part of ISO/IEC 10536 is to be used in conjunction with ISO/IEC 10536-1 and ISO/IEC 10536-2.

NOTE 1 Other types of contactless integrated circuit(s) cards, formats or interfaces, which operate at various distances, may be developed in the future, which may call for additions to be made to this part of ISO/IEC 10536 or may require other International Standards to be written.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this part of ISO/IEC 10536 are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 1177: 1985, *Information processing - Character structure for start/stop and synchronous character oriented transmission.*

ISO 7810: 1985, *Identification cards - Physical characteristics.*

ISO/IEC 7811-1: 1995, *Identification cards - Recording technique - Part 1: Embossing.*

ISO/IEC 7811-2: 1995, *Identification cards - Recording technique - Part 2: Magnetic Stripe.*

ISO/IEC 7811-3: 1995, *Identification cards - Recording technique - Part 3: Location of embossed characters on ID-1 cards.*

ISO/IEC 7811-4: 1995, *Identification cards - Recording technique - Part 4: Location of read-only magnetic tracks - Tracks 1 and 2.*

ISO/IEC 7811-5: 1995, *Identification cards - Recording technique - Part 5: Location of read-write magnetic track - Track 3.*

ISO/IEC 7812-1: 1993, *Identification cards - Identification of issuers - Part 1: Numbering system.*

ISO/IEC 7812-2: 1993, *Identification cards - Identification of issuers - Part 2: Application and registration procedures.*

ISO 7813: 1985, *Identification cards - Financial transaction cards.*

ISO 7816-1: 1987, *Identification cards - Integrated circuit(s) cards with contacts - Part 1: Physical characteristics.*

ISO 7816-2: 1988, *Identification cards - Integrated circuit(s) cards with contacts - Part 2: Dimensions and location of contacts.*

ISO 7816-3: 1989, *Identification cards - Integrated circuit(s) cards with contacts - Part 3: Electronic signals and transmission protocols.*

ISO/IEC 10536-1: 1992, *Identification cards - Contactless integrated circuit(s) cards - Part 1: Physical characteristics.*

ISO/IEC 10536-2: 1995, *Identification cards - Contactless integrated circuit(s) cards - Part 2: Dimensions and locations of coupling areas.*

3 Definitions, abbreviations and symbols

3.1 Definitions

For the purposes of this International Standard, the following definitions apply.

3.1.1 answer to reset: the period after the CICC is first energised (or reset by any other means) until the CICC completes sending its initial response to the reset or its powering from the CCD. This initial response is also called the answer to reset.

3.1.2 data transition period: the time period between the start of a data transition to the start of the next data transition. (See figure 1.)

3.1.3 differential non-return to zero: a bit coding method where a negative differential voltage is used to signal a logic level 0 and a positive differential voltage to signal a logic level of 1.

3.1.4 logic level 1: Mark (as defined in ISO 1177).

3.1.5 logic level 0: Space (as defined in ISO 1177).

3.1.6 non-return to zero: a bit coding method where a negative voltage is used to signal a logic level 0 and a positive voltage to signal a logic level of 1.

3.1.7 phase shift keying: a method of modulation achieved by varying the phase of the defined frequency received by the CICC, in a prescribed manner, from its energizing inductive field(s) in the CCD.

3.1.8 phase transition period: the time period between the middle of a phase transition from phase ϕ to ϕ' to the middle of the next phase transition. (See figure 1.)

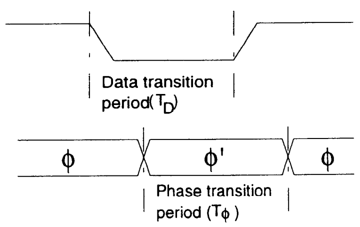

Figure 1 - Data transition period and phase transition period

3.2 Abbreviations

The following abbreviations are used in this part of ISO/IEC 10536:

ATR	Answer To Reset
CICC	Contactless Integrated Circuit(s) Card
CCD	Card Coupling Device
ID-1	Identification card of the type specified in ISO/IEC 7810: 1995
NRZ	Non-Return to Zero
PSK	Phase Shift Keying

3.3 Symbols

The following symbols apply to this part of ISO/IEC 10536:

E1-E4	As defined in ISO/IEC 10536-2
F1-F4	The fields passing through H1-H4, respectively.
H1-H4	As defined in ISO/IEC 10536-2
ϕ	Phase
t_R	Rise time between 10% and 90% of signal amplitude
t_F	Fall time between 90% and 10% of signal amplitude
T_D	Data transition period
T_ϕ	Phase transition period
V_{th}	Differential threshold input voltage
V_{hys}	Differential input hysteresis
V_{diff}	Differential voltage

4 Operating sequence for contactless integrated circuit(s) cards

This operating sequence applies to contactless integrated circuit(s) cards covered by this part of ISO/IEC 10536.

The dialogue between the CCD and the CICC is conducted through the following consecutive operations:

- activation of the CICC by the CCD powering field,
- internal reset of the CICC,
- transmission of a response from the CICC,
- subsequent information exchange between the CICC and CCD, and
- removal of the CICC from the CCD, or de-activation by the CCD.

These operations use the electronic signals and reset procedures specified in the following clauses.

5 Power Transfer

The four inductive coupling areas H1-H4 shall be excited by concentrated alternating fields F1-F4, each capable of supplying power to a CICC.

5.1 Frequency

The frequency of the alternating fields shall be 4,9152 MHz at least during ATR. The frequency of the energizing fields shall remain within ± 0,1%.

5.2 Waveform

The waveform of the alternating field shall be sinusoidal with total harmonic distortion less than 10%.

5.3 Relationship between fields

The fields passing through areas H1 and H2 may be driven from the same source but must be 180° out of phase with each other.

Likewise, the fields passing through areas H3 and H4 may be driven from the same source but be 180° out of phase with each other. The phase difference shall remain within ±10% of nominal.

Magnetic fields F1 and F3 (and hence F2 and F4) shall both be present and have a 90° phase difference at least during ATR. The phase difference shall remain within ±10% of nominal.

5.4 Power Levels

Each exciting field of the CCD shall be capable of coupling at least 150 mW of power to the CICC. The CICC shall draw no more than 150 mW from a single exciting field. The maximum power the CICC shall draw is 200 mW.

Annex A provides test methods for power transfer.

6 Communications

Communications between CICC and CCD may take place inductively via the inductive coupling areas, or capacitively via the capacitive coupling areas. In either case, only one method of data transfer shall be operational at any one time, at least during answer to reset.

6.1 Inductive data transfer

All inductive data communications shall be transmitted between the CICC and the CCD according to the descriptions in the following subclauses.

6.1.1 Communications from CICC to CCD

The CICC shall be capable of communicating to the CCD through one or more of its four inductive coupling areas H1 ... H4, whereby the alternating fields F1 ... F4 are additionally loaded to generate a subcarrier and whereby these fields are modulated by phase shift keying this subcarrier.

6.1.1.1 Subcarrier and modulation

The subcarrier shall be generated continuously with a frequency of 307,2 kHz by switching an alternating load of at least 10% of the initial load but no less than 1mW. During modulation, the phase of the subcarrier switches by 180°. This effectively defines two states for the phase.

6.1.1.2 Phase transition period

The difference between the phase transition period (T_ϕ) and the nominal data transition period (T_D) shall be less than 20% of T_D:

$$| T_\phi - T_D | / T_D < 20\%$$

6.1.1.3 Coding technique

NRZ coding shall be used for data transfer from the CICC to the CCD.

6.1.1.4 Assignments of logic level 1 and 0

When the CICC is first energized, the CCD shall determine logic level 1 for the current phase condition during the time interval t_3. After time interval t_3, each phase shift of the subcarrier shall define an inverse logical state. The time interval t_3 is defined in table 3.

6.1.2 Communications from CCD to CICC

The CICC shall be capable of communicating from the CCD through the four alternating fields F1 ... F4, whereby these fields F1 ... F4 are modulated inductively by a phase shift keying.

6.1.2.1 Modulation

During modulation, each field switches its phase (ϕ) by 90° simultaneously. This switching effectively defines two states, A and A', for the phase. Depending on the orientation of the CICC, these states are defined differently. These two alternatives are shown in figures 2 and 3.

The first alternative is:

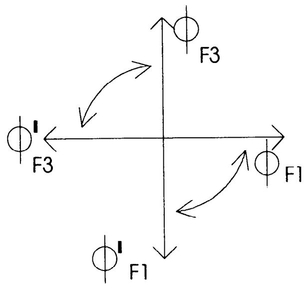

Figure 2 - Phase shifting - Alternative 1

The change in phase for this alternative is also defined in table 1.

Table 1 - Phase Shifting (Alternative 1)

State A	State A'
ϕ_{F1} $\phi_{F3} = \phi_{F1} + 90°$	$\phi'_{F1} = \phi_{F1} - 90°$ $\phi'_{F3} = \phi_{F3} + 90°$

The second alternative is:

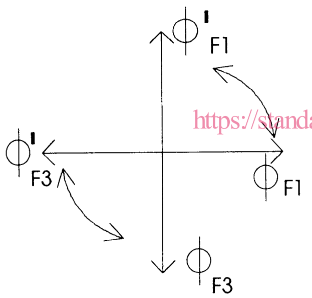

Figure 3 - Phase shifting - Alternative 2

The change in phase for this alternative is also defined in table 2.

Table 2 - Phase Shifting (Alternative 2)

State A	State A'
ϕ_{F1} $\phi_{F3} = \phi_{F1} - 90°$	$\phi'_{F1} = \phi_{F1} + 90°$ $\phi'_{F3} = \phi_{F3} - 90°$

NOTE 2 The relationship between the fields F1 ... F4 remain the same as defined in paragraph: "4.3 Relationship between fields."

6.1.2.2 Phase transition period

The difference between the phase transition period (T_{ϕ}) and the nominal data transition period (T_D) shall be less than 10% of T_D:

$$| T_{\phi} - T_D | / T_D < 10\%$$

6.1.2.3 Coding technique

NRZ coding shall be used for data transfer from the CCD to the CICC.

6.1.2.4 Assignments of logic level 1 and 0

Because the CICC operates in all four possible directions relatively to the CCD, different phase conditions may apply. When the CICC is first energized it will determine logic 1 for the current phase condition during the time interval t_2 and t_3. After time interval t_3, each phase shift of the field(s) shall define an inverse logical level. These time intervals are defined in table 3.

6.2 Capacitive data transfer

6.2.1 Relationship of the Coupling Areas

For capacitive data transfer, one pair of coupling areas is used for communication from the CICC to the CCD. This pair may be either coupling areas E1 and E2 or E3 and E4. If capacitive communication is also used from the CCD to the CICC, the other pair of coupling areas provides the communication channel from the CICC to the CCD. In both cases, the pairs of capacitive coupling areas have a differential relationship. The polarity of the capacitive coupling areas shall alternate relative to their adjacent areas. The initial state of the outer capacitive coupling area of the CICC transmitting data shall be positive.

6.2.2 Transmission characteristics

All capacitive data communications shall be transmitted between the CICC and the CCD according to the descriptions in the following subclauses.

6.2.2.1 Differential voltage

The differential voltage (V_{diff}) between the pair of capacitive coupling areas E1 and E2 or E3 and E4 shall be a maximum of 10 V and a minimum needed to generate a signal to the receiver greater than the minimum differential input threshold defined in 6.2.3.1.

6.2.2.2 Description of coding technique

The coding technique for capacitive data transfer shall be differential NRZ.

6.2.2.3 Description of data transfer technique

The transmitter communicates with the receiver by switching the differential voltage between coupling areas E1 and E2 or between E3 and E4.

6.2.2.4 Assignments of logic level 1 and 0

Logic level 1 is set during time interval t_3. After time interval t_3, each switch of the differential voltage shall define an inverse logical level. The time intervals are defined in table 3.

6.2.2.5 Slew rate

The slew rate of the differential voltage signal transmitted shall be a minimum of 0,14 V/ns.

6.2.3 Reception characteristics

All capacitive data communications shall be received between the CICC and the CCD according to the descriptions in the following subclauses.

6.2.3.1 Differential input threshold

The receiver shall be able to respond to a minimum differential input threshold (V_{th}) of ±330 mV.

6.2.3.2 Input hysteresis

The receiver shall have a minimum differential input hysteresis (noise immunity) (V_{hys}) of ±130 mV.

6.2.3.3 Slew rate

The receiver shall be able to respond to a minimum slew rate of 0,14 V/ns.

6.2.3.4 Signal width

The width of the differential voltage signal at the differential input threshold shall be at least 10 ns.

6.2.4 Initial Conditions

The CICC shall send its answer to reset on one of two pairs of capacitive plates, E1 and E2 or E3 and E4. This defines the communication channel for communication from the CICC to the CCD. For capacitive communication from the CCD to the CICC, the other pair of capacitive plates is used. The answer to reset is also used to determine the orientation of the card, if necessary.

7 Conditions for reset of the CICC

The conditions for reset of the CICC's electronics are dictated by the internal circuitry of the CICC.

When a CICC is presented to a CCD, the presence of the CICC may be indicated by the receipt of the answer to reset, by detection of an increased load on the energizing field, by mechanical means, or through other detection methods.

Subsequently, however, a reset can be accomplished by switching the powering field off and then on.

7.1 Data rate for ATR

The data transfer rate from CICC to CCD at least during the ATR shall be 9,600 b/s.

7.2 Timing Constraints

For the contactless communication system to work correctly, timing constraints must be set. Figure 4 shows timing constraints for the reset recovery time interval (t_0), the power rise time interval (t_1), the preparation time interval for data communication (t_2), the stable logic time interval (t_3), and the response time interval for answer to reset (t_4). Table 3 provides timing constraint values.

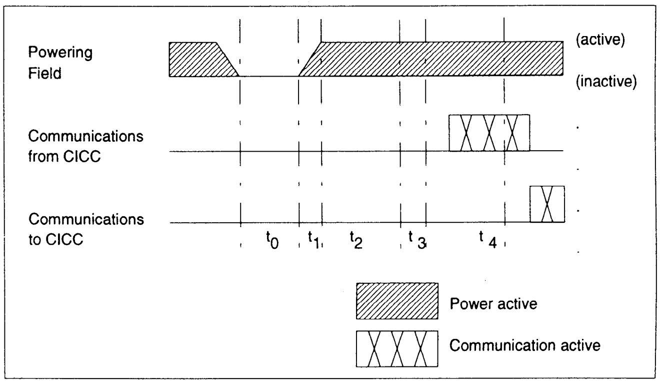

Figure 4 - Timing Constraints

Table 3 - Timing Constraint Values

Time Interval	Name	Communication		Value
		From CICC	To CICC	
t_0	reset recovery time interval	Not allowed	Not allowed	≥ 8 ms
t_1	power rise time interval	Not defined	Not defined	≤ 0,2 ms
t_2	preparation time interval	Not defined	Logic level 1	8 ms
t_3	stable logic time interval	Logic level 1	Logic level 1	2 ms
t_4	response time interval for ATR	ATR	Not defined	≤ 30 ms

7.2.1 Minimum reset recovery time interval

Should a reset be effected from the CCD by switching the powering fields off and on, a minimum reset recovery time interval t_0 shall be defined in which no energy is supplied to the CICC where

$$t_0 \geq 8{,}0 \text{ ms}$$

7.2.2 Maximum power rise time interval

The rise time for a powering field supplied by the CCD shall be defined as follows:

$$t_1 \leq 0{,}2 \text{ ms}$$

7.2.3 Preparation time interval

A preparation time interval for the CICC to become stable and be able to communicate is defined as:

$$t_2 = 8 \text{ ms}$$

7.2.4 Stable logic time interval

Before answer to reset, there will be a time interval for the logic level be held at 1. This time interval, the stable logic time interval, shall be defined as:

$$t_3 = 2 \text{ ms}$$

During this time, a CICC and CCD supporting inductive data transfer will be set to logic level 1.

7.2.5 Maximum response time interval for ATR

The CICC shall commence the ATR sequence within a specified response time interval t_4 where

$$t_4 \leq 30 \text{ ms}$$

NOTE 3 The CICC may send an ATR before the CCD has completed the preparation time interval.

8 Conditions after reset

The CICC may indicate during the ATR that it requires changes to the conditions for power levels, frequency of fields, data rate, or preferred communication methods.

Annex A
(normative)

Test methods for power transfer

A.1 Introduction

This annex describes the methods for testing power transfer from the CCD to the CICC. Power transfer with a single large coil and two small coils is tested. In addition, tests are included for the indirect measurement of the magnetic field in the inductive coupling areas.

A.2 Magnetic Field Test Circuit

Figure A.1 shows the circuit to indirectly measure the magnetic field through the voltage induced in the coil in a test card or a sense coil insert.

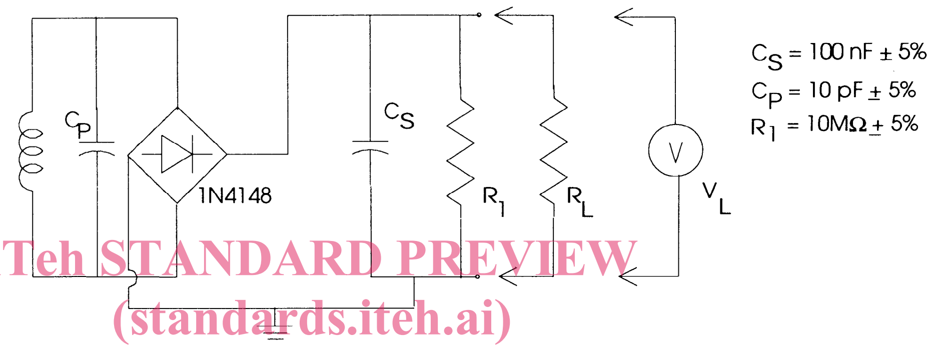

Figure A.1 - Magnetic Field Test Circuit

The values of R_L vary according to the test conditions. This test circuit is used with and without R_L. If R_L is not specified then the voltage meter will be used to test across R_1 alone.

A.3 Test Procedures

A.3.1 Single-Coil Power Transfer

For the single-coil power transfer test, the CCD and the test card (figure D.1) shall be set up as shown in figure D.7.

The test will verify that the power supplied to the surface of the test card is consistent with subclause 4.4 of the specification. All four inductive fields shall be tested.

With R_L = 330Ω ± 5%, the voltage V_L raised at R_L shall be between 7,0 V_{dc} (150 mW) and 8,1 V_{dc} (200mW) in the position as specified in the test setup.

When R_L is increased to 1MΩ ± 5%, the voltage V_L shall be less than 45 V_{dc}.

A.3.2 Flux with the Large Sense Coil

The large sense coil, sense coil #1, in the test coil insert shown in figure D.2 tests the effective flux generated around the coupling areas.

For this test, the CCD, the test card, and the sense coil insert shall be set up as shown in figure D.8. The sense coil shall be inserted between the test card and the CCD to measure the effective flux.

Both coils on the test card will be loaded using the circuit in figure A.1 with a common load R_L = 330Ω ± 5%.

The voltage raised across R_1 on the sense coil shall be more than 6,0 V_{dc}.