



# SLOVENSKI STANDARD

## SIST EN 60749-28:2017

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**Polprevodniški elementi - Metode za mehansko in klimatsko preskušanje - 28. del:  
Preskušanje občutljivosti na elektrostatično razelektritev (ESD) - Model z  
elektrostatično nabitim elementom (CDM) - Raven elementa (IEC 60749-28:2017)**

Semiconductor devices - Mechanical and climatic test methods - Part 28: Electrostatic discharge (ESD) sensitivity testing - Charged device model (CDM) - device level (IEC 60749-28:2017)

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**ICS:**

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
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EUROPEAN STANDARD

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English Version

Semiconductor devices - Mechanical and climatic test methods -  
Part 28: Electrostatic discharge (ESD) sensitivity testing -  
Charged device model (CDM) - device level  
(IEC 60749-28:2017)

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mécaniques et climatiques - Partie 28: Essai de sensibilité  
aux décharges électrostatiques (DES) - Modèle de dispositif  
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(IEC 60749-28:2017)

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elektrostatische Entladungen (ESD) - Charged Device  
Model (CDM) - Device Level  
(IEC 60749-28:2017)

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**EN 60749-28:2017****European foreword**

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IEC 60749-26 NOTE Harmonized as EN 60749-26.

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# INTERNATIONAL STANDARD



**Semiconductor devices – Mechanical and climatic test methods –  
Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device  
model (CDM) – device level**

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –  
MECHANICAL AND CLIMATIC TEST METHODS –****Part 28: Electrostatic discharge (ESD) sensitivity testing –  
Charged device model (CDM) – device level**

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This standard is based on ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002 which resulted from the merging of JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards. The co-operation of ANSI/ESDA/JEDEC is gratefully acknowledged.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2362/FDIS	47/2379/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices –Mechanical and climatic test methods*, can be found on the IEC website.

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## INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

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## SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

### Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

#### 1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex I.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

#### 2 Normative references

[SIST EN 60749-28:2017](https://standards.iteh.ai/catalog/standards/sist/e52481e9-6b81-499a-97be-0ec87e52b240/sist-en-60749-28-2017)

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There are no normative references in this document.

#### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

##### 3.1

##### **CDM ESD**

charged device model electrostatic discharge

electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

##### 3.2

##### **CDM ESD tester**

charged device model electrostatic discharge tester

equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

### 3.3

#### **dielectric layer**

thin insulator placed atop the field plate used to separate the device from the field plate

### 3.4

#### **field plate**

conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

### 3.5

#### **ground plane**

conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

### 3.6

#### **software voltage**

user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

### 3.7

#### **test condition**

#### **TC**

tester plate voltage that meets the waveform parameter conditions

Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

## 4 Required equipment

### 4.1 CDM ESD tester

#### 4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1  $\Omega$  current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1  $\Omega$  pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1  $\Omega$  resistor between the pogo pin and the ground plane, and the 50  $\Omega$  impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.