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Std 1355**

First edition
2000-07

**Information Technology –
Microprocessor Systems – Heterogeneous
InterConnect (HIC) (Low-Cost, Low-Latency
Scalable Serial Interconnect for
Parallel System Construction)**

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Abstract: Enabling the construction of high-performance, scalable, modular, parallel systems with low system integration cost is discussed. Complementary use of physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating at speeds of 10 200 Mb/s and at 1 Gb/s in copper and optic technologies, is described.

Keywords: flow control, encoding schemes, OMI/HIC, packet routing, parallelism, point-to-point serial scalable interconnect, protocols, routing fabric, serial links, serialization, silicon integration, switch chip, transaction layer, wormhole routing.

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CONTENTS

	Page
FOREWORD	8
INTRODUCTION	9
Clause	
1 Scope and object	15
2 Normative references	15
3 Definitions	17
3.1 General	17
3.2 Glossary	17
4 Physical media and logical layers	23
4.1 Physical media	23
4.2 Logical layers	24
4.3 Interaction of layers	27
4.4 Implementations defined in this International Standard	29
5 DS-SE and DS-DE	31
5.1 General	31
5.2 DS-SE: physical medium	32
5.3 DS-SE signal level	32
5.4 DS-DE: physical medium	38
5.5 DS-DE signal level	44
5.6 DS-SE and DS-DE character level	46
5.7 DS-SE and DS-DE exchange level	48
6 TS-FO-02 fiber optic link	51
6.1 Physical medium	51
6.2 Signal level	53
6.3 TS-FO character level	55
6.4 TS-FO exchange level	57
7 HS-SE-10	62
7.1 HS-SE physical medium	62
7.2 HS-SE signal level	66
7.3 HS character level (8B/12B code)	69
7.4 HS exchange level	86
8 HS-FO-10 fiber optic link	94
8.1 Physical medium	94
8.2 Signal level	97
8.3 Character level and exchange level	99
9 Common packet level	99
9.1 General discussion	99
9.2 Packet format	99
9.3 Networks and routing	100
9.4 Error detection, recovery, and reporting	101
10 Conformance criteria	101
10.1 Conformance statements	101
10.2 Definition of subsets	101

Annex A (normative) DS-DE connector specification	103
Annex B (normative) HS-SE connector specification	110
Annex C (normative) TS-FO and HS-FO connector specifications	116
Annex D (informative) Rationale	128
Annex E (informative) Switch chips, switches, and fabrics	132
Annex F (informative) Use of the transaction layer – Asynchronous transfer mode (ATM) example	134
Annex G (informative) Error handling	145
Annex H (informative) Flow control calculations	146
Annex I (informative) Synchronized channel communications	149
Annex J (informative) Example DS-SE driver circuit	152
Annex K (informative) DS-DE optional power supply recommendation	154
Annex L (informative) DS-DE fixed connector PCB recommendation	155
Annex M (informative) DS-DE cable (10 core) recommendation.....	156
Annex N (informative) DS-DE multiway connector housing recommendation.....	157
Annex O (informative) HS-SE fixed connector PCB recommendation.....	158
Annex P (informative) HS-SE cable recommendation	159
Annex Q (informative) HS-SE connector multiway housing recommendation.....	160
Annex R (informative) TS/HS-FO connector PCB and front panel cut-out recommendation .	161
Annex S (informative) TS/HS-FO fiber cable recommendation	162
Figure 1 – Protocol stack between nodes.....	23
Figure 2 – Exchange layer	26
Figure 3 – Protocol stack diagram showing interaction of layers	28
Figure 4 – Defined implementation of physical and logical layers.....	30
Figure 5 – DS-SE link signal propagation	33
Figure 6 – DS-SE timing reference model	35
Figure 7 – DS-SE link timings	36
Figure 8 – DS-SE link signal encoding	37
Figure 9 – DS-DE cable assembly twist example.....	40
Figure 10 – DE-DE extension adapter	40
Figure 11 – DS-DE fixed connector external view.....	41
Figure 12 – Multiple power connectors.....	43
Figure 13 – DS-SE/DS character encoding.....	46
Figure 14 – DS-SE/DS-DE parity coverage.....	47
Figure 15 – DS link states.....	49
Figure 16 – DS link start-up and reset.....	50
Figure 17 – TS-FO cable fibers/plugs wiring.....	52
Figure 18 – TS-FO extension adapter	52
Figure 19 – TS-FO fixed adaptor, external view and ferrule allocation.....	53
Figure 20 – TS-FO reference list.....	54
Figure 21 – TS-FO link states	58
Figure 22 – TS link start-up and reset	59

Figure 23 – TS-FO packet encoding..... 61

Figure 24 – Single braid and double braid link cables 64

Figure 25 – HS-SE cable pins/connectors wiring 65

Figure 26 – HS-SE extension adapter 65

Figure 27 – HS-SE fixed connector external view 65

Figure 28 – Input and output buffer electrical model 67

Figure 29 – Exchange level interconnection between two nodes 87

Figure 30 – Transmitter state machine controller-start-up..... 88

Figure 31 – Transmitter state machine controller-functional..... 89

Figure 32 – Transmitter state machine controller-shutdown 89

Figure 33 – Receiver state machine controller..... 90

Figure 34 – Exchange for start-up, functional and shutdown 91

Figure 35 – Exchange for bidirectional start-up 92

Figure 36 – HS-FO cable fibers/plugs wiring 95

Figure 37 – HS-FO extension adapter 96

Figure 38 – HS-FO fixed adapter, external view and ferrule allocation 96

Figure 39 – HS-FO reference link 98

Figure A.1 – DS-DE fixed connector front view..... 105

Figure A.2 – DS-DE fixed connector side view..... 106

Figure A.3 – DS-DE fixed connector top view..... 106

Figure A.4 – DS-DE connector latch..... 107

Figure A.5 – DS-DE free connector front view..... 108

Figure A.6 – DS-DE free connector side view..... 109

Figure A.7 – DS-DE free connector contact..... 109

Figure B.1 – HS-SE free connector front view 112

Figure B.2 – HS-SE free connector side view 112

Figure B.3 – HS-SE fixed connector front view 113

Figure B.4 – HS-SE fixed connector side view..... 113

Figure B.5 – HS-SE connector link..... 114

Figure B.6 – HS-SE contact interface dimensions 115

Figure C.1 – TS-FO/HS-FO link free connector 126

Figure C.2 – TS-FO/HS-FO link fixed connector..... 127

Figure F.1 – ATM network..... 134

Figure F.2 – ATM layers 136

Figure F.3 – Virtual channels and virtual paths..... 137

Figure F.4 – Example of virtual path and virtual channel switching..... 138

Figure F.5 – ATM cell header..... 139

Figure F.6 – Mapping reference model..... 140

Figure H.1 – Theoretical maximum transmission length calculation 147

Figure H.2 – Distance versus buffer size for DS and TS links 147

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Figure H.3 – Distance versus buffer size for HS-SE links	148
Figure J.1 – DS-SE pad equivalent circuit	153
Figure J.2 – Simulation input waveforms	153
Figure K.1 – Optional power supply circuit.....	154
Figure L.1 – DS-DE fixed connector PCB layout.....	155
Figure M.1 – Recommended DS-DE link cable cross-section.....	156
Figure N.1 – DS-DE connector multiway housing.....	157
Figure N.2 – DS-DE (multiway) front panel cut-out	157
Figure P.1 – Recommended HS-SE link shielded cable cross-section.....	159
Figure O.1 – Recommended HS-SE fixed connector PCB layout	158
Figure Q.1 – HS-SE multiway housing.....	160
Figure Q.2 – HS-SE (multiway) front panel cut out	160
Figure R.1 – TS/HS-FO fixed connector PCB footprint.....	161
Figure R.2 – TS/HS-FO fixed connector front panel cut-out	161
Figure S.1 – Example of TS/HS-FO fiber cable structure	162
Table 1 – Identification format for technologies	30
Table 2 – Defined implementations.....	31
Table 3 – Driver to line impedance matching table	34
Table 4 – DS-SE input capacitance.....	34
Table 5 – DS-SE timing and swings	35
Table 6 – DS-SE output skew parameters.....	37
Table 7 – Identification of multiple link interfaces	38
Table 8 – DS-DE cable color code	38
Table 9 – Electrical and mechanical characteristics and safety certification of DS-DE cable...	39
Table 10 – DS-DE link cable conductors/connectors wiring	40
Table 11 – Pin allocation of DS-DE connector	41
Table 12 – DS-DE connector modularity specifications	41
Table 13 – DS-DE environmental constraints	42
Table 14 – Optional power supply	42
Table 15 – Optional power supply load.....	42
Table 16 – Optional power supply protective device	43
Table 17 – DS-DE signal levels.....	44
Table 18 – DS-DE correspondence	45
Table 19 – Attribution of attenuation budget	45
Table 20 – Attribution of skew budget	45
Table 21 – Terminator character codings	47
Table 22 – Link control character codings	47
Table 23 – Summary of main optical characteristics of TS-FO fibers	51
Table 24 – TS-FO connector modularity specifications	52
Table 25 – TS-FO signal allocation	53
Table 26 – TS-FO environmental constraints.....	53
Table 27 – TS-FO recommended transceiver characteristics	54

Table 28 – TS-FO link performance specification	55
Table 29 – Symbols allocated for character coding of data values	56
Table 30 – Symbols for control characters	56
Table 31 – Coding of control characters	57
Table 32 – Coding of INIT	57
Table 33 – HS-SE-10 links general characteristics	62
Table 34 – PCB track characteristics	62
Table 35 – Physical characteristics of a single coaxial cable	63
Table 36 – Electrical characteristics of a single coaxial cable	63
Table 37 – Mechanical performance and safety certification of link cables	64
Table 38 – Pin allocation of HS-SE connector	66
Table 39 – HS-SE environmental constraints	66
Table 40 – HS-SE environmental constraints	66
Table 41 – Operating rates for HS-SE-10 links	66
Table 42 – Attribution of attenuation budget	68
Table 43 – Driver side line logic levels for $V_{DD} = 3.3$ V (nominal)	68
Table 44 – Driver side line logic levels for $V_{DD} = 5.0$ V (nominal)	68
Table 45 – Driver side line swing when ac coupled into 50 Ω termination	68
Table 46 – Receiver electrical characteristics	69
Table 47 – Data characters	72
Table 48 – Control characters	83
Table 49 – Reserved L_chars for exchange level functions	87
Table 50 – Time-out values	92
Table 51 – Summary of main optical characteristics of HS-FO fibers	95
Table 52 – THS-FO connector modularity specifications	95
Table 53 – HS-FO signal allocation	96
Table 54 – HS-FO environmental constraints	96
Table 55 – HS-FO recommended transceiver characteristics for multimode fiber	97
Table 56 – HS-FO recommended transceiver characteristics for single mode fiber	97
Table 57 – HS-FO link performance specification	98
Table 58 – End_of_packet markers	100
Table 59 – Codes for EOP markers	100
Table 60 – Conformance identifications for connectors	101
Table 61 – Conformance identifications for link cables	101
Table 62 – Conformance identifications for link cable assemblies	102
Table 63 – Common identifications for link interfaces	102
Table A.1 – DS-DE connector requirements	103
Table B.1 – HS-SE connector requirements	110

Table C.1 – TS-FO and HS-FO (multimode) connector requirements.....	116
Table C.2 – Performance and environmental specification for TS-FO and HS-FO (multimode) connector.....	119
Table C.3 – HS-FO (single-mode) connector requirements.....	121
Table C.4 – Performance and environmental specification for HS-FO (single-mode) connector.....	124
Table C.5 – Color coding of TS/HS-FO connectors.....	127
Table J.1 – Parameter spread for DS-SE link driver.....	152
Table L.1 – PCB details for DS-DE connector attachment.....	155
Table M.1 – Recommended DS-DE link cable specification.....	156
Table P.1 – Recommended HS-SE cable specifications.....	159

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INFORMATION TECHNOLOGY – MICROPROCESSOR SYSTEMS – HETEROGENEOUS INTERCONNECT (HIC) (LOW-COST, LOW-LATENCY SCALABLE SERIAL INTERCONNECT FOR PARALLEL SYSTEM CONSTRUCTION)

FOREWORD

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International Standards are drafted in accordance with ISO/IEC Directives, Part 3.

Annexes A, B and C form an integral part of this standard.

Annexes D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R and S are for information only.

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INTRODUCTION

(This introduction is not a normative part of ISO/IEC 14575:2000, but is included for information only.)

The construction of high-performance systems with parallel communications, parallel processing, and/or parallel I/O demands a fast, low-cost, low-latency interconnect. It must be fast and low-latency, otherwise it will be the limiting factor in system performance; and it must be low-cost, or it will dominate the system cost. It must also scale well in both performance and cost relative to the system size, otherwise highly parallel systems will be limited in performance or too expensive. Existing standards do not meet these criteria, because they are designed for communication over long distances (which incurs high costs), or because they aim at the extreme of currently achievable performance (which again increases costs), or because they are based on a restricted model such as a bus, which limits overall performance and scalability. A detailed rationale for this standard is given in annex D.

This standard has been developed to complement recent technical developments of highly integrated, low-power interconnect technology implemented in high-volume commodity VLSI processes, and to exploit the simplifications in encodings and protocols resulting from the use of relatively reliable media over relatively short distances. Aspects of the baseline for this standard have their origins in work on parallel systems, which has taken place in a number of ESPRIT projects. In particular, the routing strategy was established in the PUMA project, and the DS-Links were developed partially in the GP MIMD project. Work at interconnect for high-performance mainframe computers at Bull led to the development of the gigabit link technology implemented in Bi-CMOS and CMOS processes. More recently, these developments, together with corresponding optical technology, have been brought together in the OMI/HIC Project (Open Microprocessor Systems Initiative – High Performance Heterogeneous Interconnect – ESPRIT 7252).

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