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Information Technology – Microprocessor Systems – Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction)

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Abstract: Enabling the construction of high-performance, scalable, modular, parallel systems with low system integration cost is discussed. Complementary use of physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating at speeds of 10 200 Mb/s and at 1 Gb/s in copper and optic technologies, is described.

Keywords: flow control, encoding schemes, OMI/HIC, packet routing, parallelism, point-to-point serial scalable interconnect, protocols, routing fabric, serial links, serialization, silicon integration, switch chip, transaction layer, wormhole routing.

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International Standard ISO/IEC 14575 was prepared by subcommittee 26: Microprocessor systems, of ISO/IEC joint technical committee 1: Information technology.

International Standards are drafted in accordance with ISO/IEC Directives, Part 3.

Annexes A, B and C form an integral part of this standard.

Annexes D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R and S are for information only.

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INTRODUCTION

(This introduction is not a normative part of ISO/IEC 14575:2000, but is included for information only.)

The construction of high-performance systems with parallel communications, parallel processing, and/or parallel I/O demands a fast, low-cost, low-latency interconnect. It must be fast and low-latency, otherwise it will be the limiting factor in system performance; and it must be low-cost, or it will dominate the system cost. It must also scale well in both performance and cost relative to the system size, otherwise highly parallel systems will be limited in performance or too expensive. Existing standards do not meet these criteria, because they are designed for communication over long distances (which incurs high costs), or because they aim at the extreme of currently achievable performance (which again increases costs), or because they are based on a restricted model such as a bus, which limits overall performance and scalability. A detailed rationale for this standard is given in annex D.

This standard has been developed to complement recent technical developments of highly integrated, low-power interconnect technology implemented in high-volume commodity VLSI processes, and to exploit the simplifications in encodings and protocols resulting from the use of relatively reliable media over relatively short distances. Aspects of the baseline for this standard have their origins in work on parallel systems, which has taken place in a number of ESPRIT projects. In particular, the routing strategy was established in the PUMA project, and the DS-Links were developed partially in the GP MIMD project. Work at interconnect for high-performance mainframe computers at Bull led to the development of the gigabit link technology implemented in Bi-CMOS and CMOS processes. More recently, these developments, together with corresponding optical technology, have been brought together in the OMI/HIC Project (Open Microprocessor Systems Initiative – High Performance Heterogeneous Interconnect – ESPRIT 7252).

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