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**Element z ugnezdenim substratom - Rodovna specifikacija - Preskusna metoda**

Device embedded substrate - Generic specification - Test method

Trägermaterial mit eingebetteten Bauteilen - Teil 1-1: Fachgrundspezifikation - Prüfverfahren

Substrat avec appareil(s) intégré(s) - Partie 1-1: Spécification générique - Méthodes d'essai

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EUROPEAN STANDARD

**EN 62878-1-1**

NORME EUROPÉENNE

EUROPÄISCHE NORM

July 2015

ICS 31.180; 31.190

English Version

Device embedded substrate -  
Part 1-1: Generic specification - Test methods  
(IEC 62878-1-1:2015)

Substrat avec appareil(s) intégré(s) -  
Partie 1-1: Spécification générique - Méthodes d'essai  
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Trägermaterial mit eingebetteten Bauteilen -  
Teil 1-1: Fachgrundspezifikation - Prüfverfahren  
(IEC 62878-1-1:2015)

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Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels**

**EN 62878-1-1:2015****European foreword**

The text of document 91/1248/FDIS, future edition 1 of IEC 62878-1-1, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62878-1-1:2015.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2016-03-24
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2018-06-24

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60068-1	NOTE	Harmonized as EN 60068-1.
IEC 60068-2-6	NOTE	Harmonized as EN 60068-2-6.
IEC 60068-2-14	NOTE	Harmonized as EN 60068-2-14.
IEC 60068-2-20	NOTE	Harmonized as EN 60068-2-20.
IEC 60068-2-21	NOTE	Harmonized as EN 60068-2-21.
IEC 60068-2-30	NOTE	Harmonized as EN 60068-2-30.
IEC 60068-2-38	NOTE	Harmonized as EN 60068-2-38.
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IEC 60068-2-66	NOTE	Harmonized as EN 60068-2-66.
IEC 60068-2-78	NOTE	Harmonized as EN 60068-2-78.
IEC 60068-2-80	NOTE	Harmonized as EN 60068-2-80.
IEC 61189-1	NOTE	Harmonized as EN 61189-1.
IEC 61189-2	NOTE	Harmonized as EN 61189-2.
IEC 61189-11	NOTE	Harmonized as EN 61189-11.
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IEC 61190-1-3	NOTE	Harmonized as EN 61190-1-3.
IEC 62137-1-2	NOTE	Harmonized as EN 62137-1-2.
IEC 62137-1-3	NOTE	Harmonized as EN 62137-1-3.
IEC 62421	NOTE	Harmonized as EN 62421.
ISO 291	NOTE	Harmonized as EN ISO 291.

ISO 2409	NOTE	Harmonized as EN ISO 2409.
ISO 3611	NOTE	Harmonized as EN ISO 3611.
ISO 4957	NOTE	Harmonized as EN ISO 4957.
ISO 9445-1	NOTE	Harmonized as EN ISO 9445-1.
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ISO 9455 Series	NOTE	Harmonized as EN ISO 9455 Series.
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## Annex ZA (normative)

### Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: [www.cenelec.eu](http://www.cenelec.eu)

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60068-2-1	-	Environmental testing - Part 2-1: Tests - Test A: Cold	EN 60068-2-1	-
IEC 60068-2-2	-	Environmental testing - Part 2-2: Tests - Test B: Dry heat	EN 60068-2-2	-
IEC 60194	-	Printed board design, manufacture and assembly - Terms and definitions	EN 60194	-
IEC 61189-3	-	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 3: Test methods for interconnection structures (printed boards)	EN 61189-3	-
IEC/TS 62878-2-4	2015	Device embedded substrate - Part 2-4: Guidelines - Test element groups (TEG)	-	-



IEC 62878-1-1

Edition 1.0 2015-05

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE



**Device embedded substrate –**  
**Part 1-1: Generic specification – Test methods**

**Substrat avec appareil(s) intégré(s) –**  
**Partie 1-1: Spécification générique – Méthodes d'essai**

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## CONTENTS

FOREWORD.....	5
1 Scope.....	7
2 Normative references .....	7
3 Terms, definitions and abbreviations .....	7
3.1 Terms and definitions.....	7
3.2 Abbreviations.....	7
4 Test methods.....	8
4.1 General.....	8
4.2 Visual inspection and micro-sectioning.....	8
4.2.1 General .....	8
4.2.2 Visual inspection .....	8
4.2.3 Micro-sectioning .....	8
4.2.4 Lack of conductor and residue of conductor.....	10
4.2.5 Land dimension and land width (annular ring).....	10
4.3 Electrical tests .....	13
4.3.1 Conductor resistance.....	13
4.3.2 Through hole and build-up via .....	14
4.3.3 Withstanding current of embedded device connection.....	15
4.3.4 Withstanding voltage in embedded boards.....	17
4.3.5 Insulation resistance.....	19
4.3.6 Conduction and insulation of circuit.....	20
4.4 Mechanical tests.....	20
4.4.1 Pulling strength of conductor.....	20
4.4.2 Pulling strength of un-plated through hole.....	21
4.4.3 Pulling strength of plated through hole.....	22
4.4.4 Pulling strength of pad of land pattern .....	22
4.4.5 Adhesivity of plated foil.....	23
4.4.6 Adhesivity of solder resist and symbol mark.....	24
4.4.7 Hardness of painted film (solder resist and symbol mark).....	28
4.5 Environmental tests .....	29
4.5.1 General .....	29
4.5.2 Vapour phase thermal shock .....	30
4.5.3 High temperature immersion tests .....	30
4.5.4 Resistance to humidity.....	31
4.6 Mechanical environmental test – Resistance to migration .....	34
4.6.1 General .....	34
4.6.2 Equipment .....	34
4.6.3 Specimen .....	35
4.6.4 Test condition .....	35
5 Shipping inspection .....	36
5.1 General.....	36
5.2 Electrical test.....	37
5.2.1 General .....	37
5.2.2 Test of conductor pattern not connected to an embedded component.....	38
5.2.3 Test on the pattern having a passive component and a conductor pattern.....	40



5.2.4	Test of a circuit having both active component(s) and a conductor pattern.....	43
5.2.5	Test of a circuit having connections of both individual passive component(s) and conductor pattern.....	46
5.2.6	Test of a circuit having an embedded component which cannot be checked from the surface and a conductor pattern.....	47
5.3	Internal transparent test.....	47
5.4	Visual test.....	47
Annex A (informative) Related test methods .....		49
Bibliography.....		52
Figure 1 – Measuring items of the micro-sectioned through hole structure .....		9
Figure 2 – Measuring items of the micro-sectioned device embedded board with build-up structure .....		9
Figure 3 – Measurement of land dimension.....		11
Figure 4 – Build-up land measurement.....		12
Figure 5 – Conductor resistance measurement .....		14
Figure 6 – Relationship between current, conductor width and thickness and temperature rise .....		17
Figure 7 – Adhesivity of plated film .....		24
Figure 8 – Single cutting tool .....		25
Figure 9 – Cutter knife .....		25
Figure 10 – Multiple blade cutter.....		26
Figure 11 – Equal-distance spacer with guide.....		26
Figure 12 – Cutting using a single cutting tool or a cutting knife.....		27
Figure 13 – Cross-cut test.....		28
Figure 14 – Coated film hardness test.....		29
Figure 15 – Temperature and humidity cycles .....		33
Figure 16 – Device embedded board for shipping inspection.....		36
Figure 17 – Typical circuit construction of device embedded board .....		37
Figure 18 – Examples of evaluation levels of electrical test.....		39
Figure 19 – Circuit construction not connected to embedded component .....		39
Figure 20 – Circuit construction which is capable of independent check.....		40
Figure 21 – Circuit construction for parallel connection of passive components.....		42
Figure 22 – Circuit construction for series connection of passive components.....		43
Figure 23 – Circuit construction of embedded diode.....		44
Figure 24 – Circuit construction of transistor circuit.....		44
Figure 25 – Circuit construction of a conductor pattern with embedded IC and LSI .....		45
Figure 26 – Circuit construction composed of a passive component and an active component.....		46
Figure 27 – Circuit construction of embedded components having no connection terminal on the surface .....		47
Table 1 – Test items, characteristics and observations of micro-sectioned specimens .....		9
Table 2 – Test method for coplanarity around the land pattern .....		12
Table 3 – Characteristics and test methods for conductor resistance .....		15

Table 4 – Withstanding current and test methods .....	16
Table 5 – Withstanding voltage and test methods .....	18
Table 6 – Criteria and test methods for insulation resistance .....	20
Table 7 – Characteristics and test method of pulling strength of conductor .....	21
Table 8 – Dimensions of land, hole and conductor .....	22
Table 9 – Characteristics and test methods of pulling strength of plated through hole .....	22
Table 10 – Specification and test method of pad pulling strength of land pattern .....	23
Table 11 – High and low temperature characteristics and tests .....	30
Table 12 – Thermal shock characteristics and test methods .....	30
Table 13 – Thermal shock (high temperature immersion test) .....	31
Table 14 – Measuring environment .....	31
Table 15 – Thermal shock (high temperature immersion tests) .....	31
Table 16 – Resistance to humidity characteristics and test methods .....	34
Table 17 – Resistance to migration characteristics and test methods .....	35
Table 18 – Applicable items of shipping inspection .....	37
Table A.1 – Related test methods .....	49

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

## DEVICE EMBEDDED SUBSTRATE –

## Part 1-1: Generic specification – Test methods

## FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 62878-1-1 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/1248/FDIS	91/1260/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62878, published under the general title *Device embedded substrate*, can be found on the IEC website.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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## DEVICE EMBEDDED SUBSTRATE –

### Part 1-1: Generic specification – Test methods

#### 1 Scope

This part of IEC 62878 specifies the test methods of passive and active device embedded substrates. The basic test methods of printed wiring substrate materials and substrates themselves are specified in IEC 61189-3.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

#### 2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[SIST EN 62878-1-1:2015](https://standards.iteh.ai/catalog/standards/sist/97cba642-3390-47d5-a4d9-1add9766/iec-62878-1-1-2015)

<https://standards.iteh.ai/catalog/standards/sist/97cba642-3390-47d5-a4d9-1add9766/iec-62878-1-1-2015>  
IEC 60068-2-1, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60068-2-2, *Environmental testing – Part 2-2: Tests – Test B: Dry heat*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61189-3, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 3: Test methods for interconnection structures (printed boards)*

IEC TS 62878-2-4:2015, *Device embedded substrate – Part 2-4 – Guidelines – Test element groups (TEG)*

#### 3 Terms, definitions and abbreviations

##### 3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

##### 3.2 Abbreviations

AABUS as agreed between user and supplier

AOI automated optical inspection

LSI large scale integration

## 4 Test methods

### 4.1 General

This clause is given for guidance only. The test shall be carried out at the standard air conditions (or simply stated as standard environment):

Temperature	Relative humidity	Atmospheric pressure
15°C to 35°C	25 % to 75 %	86 kPa to 106 kPa

### 4.2 Visual inspection and micro-sectioning

#### 4.2.1 General

Visual inspection and micro-sectioning of multi-layer printed wiring boards are specified in 4.2.2 and 4.2.3.

#### 4.2.2 Visual inspection

Visual inspection consists of checking the appearance, finish, and pattern of specimens using the naked eye or a magnifying glass in reference to its individual specification. The test result shall be as agreed between user and supplier (hereafter referred as AABUS).

#### 4.2.3 Micro-sectioning

Micro-sectioning is to check the state, appearance, and dimensions according to individual specifications of the plated through hole, the via in the build-up layer, the conductor, the interlayer distance, the conductor distance, and the connections to the embedded device. The specimen is mounted in epoxy or polyester resin and the specimen is cross-sectioned and polished for observation. The evaluation of the results shall be AABUS. The equipment, material, specimen and test are specified in a) to d).

##### a) Equipment

An industrial microscope capable of measuring plated film thicknesses with an accuracy of 0,001 mm.

##### b) Material

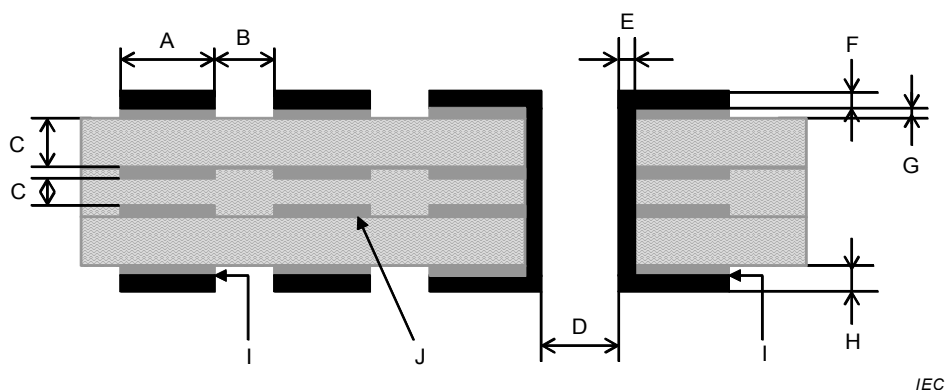
Materials used in this test are releasing agent, moulding resin, polishing cloth or paper (#180, #400, #1 000, etc.) with the option to use polishing materials (alumina or chromium oxide).

##### c) Specimen

A specimen is cut from the product to an appropriate size sufficient for observation and mounted in moulding resin. The cut surface is then polished with polishing cloth/paper starting from coarse to fine using a rotating felt surface and the above mentioned polishing material. The polishing face shall be within an angle of 85° to 95° to the layer to be observed. The diameter of the plated film of the through hole and of the vias in the build-up layer observed by micro-sectioning shall be no less than 90 % of the previously observed hole diameter. Etch the specimen if the boundary of the plating needs to be clarified after polishing.

##### d) Test

The test consists of observing the items specified in the individual specifications by means of a microscope of specified magnification. Figure 1 illustrates the test items for the through hole to check the micro-sectioned faces, and Figure 2 for the build-up structure and embedded devices. Table 1 gives the characteristics and observation items of the test.



IEC

**Key**

- |   |                                       |   |                                 |
|---|---------------------------------------|---|---------------------------------|
| A | Conductor width                       | F | Conductor plated film thickness |
| B | Conductor gap                         | G | Thickness of copper foil        |
| C | Insulation layer thickness            | H | Conductor thickness             |
| D | Hole diameter                         | I | Boundary of plated film         |
| E | Plated film thickness of through hole | J | Internal circuit                |

**Figure 1 – Measuring items of the micro-sectioned through hole structure**

IEC

**Key**

- |   |  |
|---|--|
| A | Distance between conductor and embedded device |
| B | Device embedding layer                         |

**Figure 2 – Measuring items of the micro-sectioned device embedded board with build-up structure****Table 1 – Test items, characteristics and observations of micro-sectioned specimens**

No	Test item	Characteristics and observation
1	Conductor width (inner layer, outer layer)	– Upper conductor width – Lower conductor width – Etch factor
2	Conductor gap (inner layer, outer layer)	– Minimum conductor gap
3	Insulation layer thickness/conductor gap	– Minimum insulation layer/minimum conductor gap – Delamination – Measling – Crazing
4	Hole diameter and land width	– Hole diameter – Land width