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Polprevodniški elementi - Mehanske in klimatske preskusne metode - 26. del: Preskušanje občutljivosti na elektrostatične izpraznitve (ESD) - Model človeškega telesa (HBM)

Semiconductor devices - Mechanical and climatic test methods -- Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

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Halbleiterbauelemente – Mechanische und klimatische Prüfverfahren -- Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM)

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Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques -- Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM)

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Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

(IEC 60749-26:2013)

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM) (CEI 60749-26:2013) Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM) (IEC 60749-26:2013)

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Foreword

This document (EN 60749-26:2014) consists of the text of IEC 60749-26:2013 prepared by IEC/TC 47 "Semiconductor devices", in collaboration with Technical Committee 101.

The following dates are fixed:

latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement

 latest date by which the national standards conflicting with the document have to be withdrawn

This document supersedes EN 60749-26:2006.

EN 60749-26:2014 includes the following significant technical changes with respect to EN 60749-26:2006:

- a) descriptions of oscilloscope and current transducers have been refined and updated;
- b) the HBM circuit schematic and description have been improved;
- c) the description of stress test equipment qualification and verification has been completely rewritten;
- d) qualification and verification of test fixture boards has been revised;
- e) a new section on the determination of ringing in the current waveform has been added;
- f) some alternate pin combinations have been included;
- g) allowance for non-supply pins to stress to a limited number of supply pin groups (associated non-supply pins) and allowance for non-supply to non-supply (i.e., I/O to I/O) stress to be limited to a finite number of 2 pin pairs (coupled non-supply pin pairs);
- h) explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

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Annex ZA (normative)

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The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu

<u>Publication</u>	<u>Year</u>	<u>Title</u>	EN/HD	<u>Year</u>
IEC 60749-27	-	Semiconductor devices - Mechanical and climatic test methods - Part 27: Electrostatic discharge (ESD) sensitivity testing - Machine model (MM)	EN 60749-27	-

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NORME INTERNATIONALE



Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

SIST EN 60749-26:2014

Dispositifs à semiconducteurs — Méthodes d'essais mécaniques et climatiques – Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle du corps humain (HBM)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

FOREWORD

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International Standard IEC 60749-26 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with technical committee 101.

This third edition cancels and replaces the second edition published in 2006. This edition constitutes a technical revision. This standard is based upon ANSI/ESDA/JEDEC JS-001-2010. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association.

NOTE ANSI/ESDA/JEDEC JS-001 resulted from the merging of JESD22-A114F and ANSI/ESD STM5.1.

This edition includes the following significant technical changes with respect to the previous edition:

- a) descriptions of oscilloscope and current transducers have been refined and updated;
- b) the HBM circuit schematic and description have been improved;

- c) the description of stress test equipment qualification and verification has been completely re-written;
- d) qualification and verification of test fixture boards has been revised;
- e) a new section on the determination of ringing in the current waveform has been added;
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- h) explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

The text of this standard is based on the following documents:

FDIS	Report on voting	
47/2160/FDIS	47/2167/RVD	

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEO 60749 series, published under the general title Semiconductor devices – Mechanical and climatic test methods, can be found on the IEC website.

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The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IECT web osite 2 under "http://webstore.iec.ch" in the data related to the specific publication. At this date the publication will be d-8914

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- · reconfirmed,
- · withdrawn.
- replaced by a revised edition, or
- amended.

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. The HBM and MM test methods produce similar but not identical results; unless otherwise specified, this test method is the one selected.

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2 Normative references

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The following documents ain whole or in partnare normatively referenced in this document and are indispensable for its applications. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-27, Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3 1

associated non-supply pin

non-supply pin (typically an I/O pin) associated with a supply pin group

Note 1 to entry: A non-supply pin is considered to be associated with a supply pin group if either:

- a) The current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect (high/low impedance) to that non-supply pin.
- b) A parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

3.2

component

item such as a resistor, diode, transistor, integrated circuit or hybrid circuit

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3.3

component failure

condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters

3.4

coupled non-supply pin pair

two pins that have an intended direct current path (such as a pass gate or resistors, such as differential amplifier inputs, or low voltage differential signaling (LVDS) pins), including analogue and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP DP/CCN DN etc.)

3.5

data sheet parameters

static and dynamic component performance data supplied by the component manufacturer or supplier

3.6

withstand voltage

highest voltage level that does not cause device failure

Note 1 to entry: The device passes all tested lower voltages (see failure Window).

3.7

failure window iTeh STANDARD PREVIEW

intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range

Note 1 to entry: A component with a failure window may pass a 500 V test, fail a 1 000 V test and pass 2 000 V test. The withstand voltage of this device is 500 V. EN 60749-26:2014

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3.8 be5f8f656ee2/sixthuman body model electrostatic discharge

HBM ESD

ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being to a grounded device

3.9

HBM ESD tester

HBM simulator

equipment that applies an HBM ESD to a component

3.10

I_{ps}

peak current value determined by the current at time t_{max} on the linear extrapolation of the exponential current decay curve, based on the current waveform data over a 40 nanosecond period beginning at t_{max}

SEE: Figure 2 a).

3.11

I_{psmax}

highest current value measured including the overshoot or ringing components due to internal test simulator RLC parasitics

SEE: Figure 2 a).

3.12

no connect pin

package interconnection that is not electrically connected to a die