Designation: F 1810 – 97 (Reapproved 2002)

Standard Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers[1]

This standard is issued under the fixed designation F 1810; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method describes the technique to count the density of surface defects in silicon wafers by microscopic analysis.

NOTE 1—Practical use of a defect counting method requires an assumption be made that defects are randomly distributed on the surface. If this assumption is not met, the accuracy and precision of this test method will be diminished.

1.2 Application of this test method is limited to specimens that have discrete, identifiable artifacts on the surface of the silicon sample. Typical samples have been preferentially etched according to Guide F 1809 or epitaxially deposited, forming defects in a silicon layer structure.

1.3 Wafer thickness and diameter for this test method is limited only by the range of microscope stage motions available.

1.4 This test method is applicable to silicon wafers with defect density between 0.01 and 10 000 defects per cm^2.

NOTE 2—The commercially significant defect density range is between 0.01 to 10 defects per cm^2, but this test method extends to higher defect levels due and improved statistical sampling obtained with higher counts.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 1241 Terminology of Silicon Technology[2]

F 1725 Practice for Analysis of Crystallographic Perfection of Silicon Ingots[2]

F 1726 Practice for Analysis of Crystallographic Perfection of Silicon Wafers[2]

F 1727 Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers[2]

F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon[2]

3. Terminology

3.1 Definitions of terms related to silicon technology are found in Terminology F 1241.

4. Summary of Test Method

4.1 Selected and prepared samples for this test used Practice F 1725, F 1726 or F 1727. The defect to be analyzed is exposed using a specific etching solution suggested in Guide F 1809.

4.2 Align the wafer on a microscope stage, inspect according to predefined inspection pattern and count specific defects distinguished by shape or size.

4.3 The basic inspection pattern is a single diametric scan though the center point of the wafer.

4.4 The starting and ending points of the scan pattern are 5 mm from the edges of the wafer. Fig. 1 represents the characteristics of the pattern.

4.5 The complete inspection pattern of this test method is based upon the combination of four separate scans across different diameters.

5. Significance and Use

5.1 Defects on or in silicon wafers may adversely affect device performance and yield.

5.2 Crystal defect analysis is a useful technique in troubleshooting device process problems. The type, location, and density of defects counted by this test method may be related to the crystal growth process, surface preparation, contamination, or thermal history of the wafer.

5.3 This test method is suitable for acceptance testing when used with referenced standards.

6. Interferences

6.1 Improper identification of defects is possible during the counting process.

6.1.1 Contamination not removed by cleaning procedures or deposited following cleaning, may become visible after preferential etching.

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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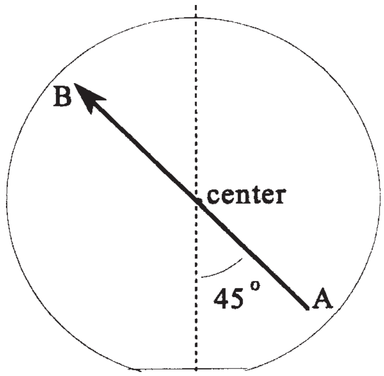
[2] *Annual Book of ASTM Standards*, Vol 10.05.



NOTE 1—Begin scan 5 mm from the edge.

FIG. 1 The Basic Microscopic Inspection Scan Pattern

6.1.2 Insufficient agitation during the preferential etching process may cause artifacts that may be mistaken as crystallographic defects.

6.2 The accuracy of the defect density calculation is directly affected by calibration of the area of the microscope field of view.

6.3 The defect density determined by this test method requires an assumption be made that defects are randomly distributed on the surface. Nonuniform patterns of defects alter the defect density measurement by their size and location.

6.4 Multiple scan patterns intersect at the center of the wafer. If a defect is found at this single, common point, it is counted more than once and shall alter the accuracy.

7. Apparatus

7.1 *Nonmetallic Vacuum Pickup Tool*, of suitable material such as quartz or TFE-fluorocarbon. The pickup tool shall be constructed so that no metal can contact the specimen wafer.

7.2 *Optical Microscope*, equipped with interference contrast attachment.

NOTE 3—Nomarski differential interference contrast is an example of interference contrast.

7.2.1 *Eyepiece and Objective Lens*, in combination shall give a magnification range of approximately 100× to 400× magnification of the specimen. The dimension of the field of view at each magnification option is calibrated to allow defect density calculations.

7.2.2 *Graduated Metric X-Y Microscope Stage* is used for sample positioning.

8. Sampling

8.1 Specimens shall be selected to represent the lot to be tested as specified in producer-consumer agreements.

9. Procedure

9.1 *Four Scan Inspection Pattern:*

9.1.1 Place the specimen wafer onto the microscope inspection stage. Handle wafers only with a clean nonmetallic vacuum pickup tool to avoid scratching or contaminating the surface.

9.1.2 Place the specimen such that a single linear motion of the stage (either x or y) allows counting of defects contained in the field of view along the path labeled AB in Fig. 1. Points A and B are found 5 mm from the wafer edge and the line AB is rotated 45° from the location of the major locating flat or notch. Alternative edge exclusion positions are acceptable with the agreement of the parties involved.

9.1.3 Scan the path and record the classification and numbers of the defects observed during the scan. Refer to descriptions and pictures in Guide F 1809.

9.1.4 Rotate the wafer by 45° on the microscope stage and repeat 9.1.3 for the second scan. Refer to Fig. 2 for improved definition of the scan pattern.

9.1.5 Rotate the wafer by 45° on the microscope stage and repeat 9.1.3 for the third and then the fourth scans.

9.2 *Defect Density Calculation:*

9.2.1 Count each defect class separately for each diameter scanned. Calculate the total area inspected by multiplying four (4) times the calibrated width of the field of view in centimeters by the length of the scan in centimeters. The length (L) is the wafer diameter (D) minus twice the edge exclusion (E),

$$[L = D - (2 \times E)]$$

The density is the defect count divided by the total area.

NOTE 4—When a scan intersects a flat, notch or laser mark, the total area must be adjusted according to the reduced length of the affected scans. Failure to adjust the area results in inaccuracy.

10. Report

10.1 Report the following information:

10.1.1 Date of test, laboratory and operator,

10.1.2 Identification of the specimen wafer, conductivity type, orientation, and diameter,

10.1.3 Specimen history; thermal cycle, preferential etchant formulation, thickness removal during preferential etching,

10.1.4 Inspection conditions; magnification, and total area inspected, and

10.1.5 Defect density and precision by defect classification.

11. Precision and Bias

11.1 *Precision*—The multi laboratory precision of this test method was established through a round-robin experiment. Seven (7) wafers with randomly distributed oxidation induced stacking faults were analyzed by sixteen (16) laboratories over eleven (11) diameter scans. Repeatability and reproducibility of this test method were calculated using two sets of four scan measurements from each laboratory and wafer. The wafer samples were prepared according to Practice F 1727 and etched with Wright Etch according to Guide F 1809.

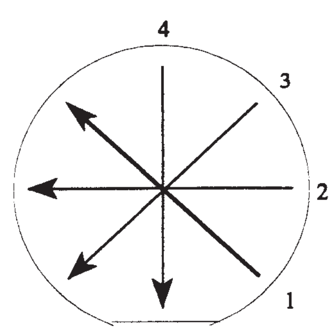


FIG. 2 Four Scan, Multiple Microscopic Inspection Pattern.