# ETSI TS 101 271 V1.1.1 (2009-01)

*Technical Specification*

**Access Terminals Transmission and Multiplexing (ATTM);
Access transmission system on metallic pairs;
Very High Speed digital subscriber line system (VDSL2);
[ITU-T Recommendation G.993.2 modified]**

Reference

DTS/ATTM-06003

Keywords

VDSL, access, modem, transmission, xDSL

***ETSI***

650 Route des Lucioles
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C
Association à but non lucratif enregistrée à la
Sous-Préfecture de Grasse (06) N° 7803/88



***Important notice***

Individual copies of the present document can be downloaded from:
http://www.etsi.org

The present document may be made available in more than one electronic version or in print. In any case of existing or perceived difference in contents between such versions, the reference version is the Portable Document Format (PDF). In case of dispute, the reference shall be the printing on ETSI printers of the PDF version kept on a specific network drive within ETSI Secretariat.

Users of the present document should be aware that the document may be subject to revision or change of status. Information on the current status of this and other ETSI documents is available at
http://portal.etsi.org/tb/status/status.asp

If you find errors in the present document, please send your comment to one of the following services:
http://portal.etsi.org/chaircor/ETSI_support.asp

# Contents

# Intellectual Property Rights

IPRs essential or potentially essential to the present document may have been declared to ETSI. The information pertaining to these essential IPRs, if any, is publicly available for **ETSI members and non-members**, and can be found in ETSI SR 000 314: *"Intellectual Property Rights (IPRs); Essential, or potentially Essential, IPRs notified to ETSI in respect of ETSI standards"*, which is available from the ETSI Secretariat. Latest updates are available on the ETSI Web server (http://webapp.etsi.org/IPR/home.asp).

Pursuant to the ETSI IPR Policy, no investigation, including IPR searches, has been carried out by ETSI. No guarantee can be given as to the existence of other IPRs not referenced in ETSI SR 000 314 (or the updates on the ETSI Web server) which are, or may be, or may become, essential to the present document.

# Foreword

This Technical Specification (TS) has been produced by ETSI Technical Committee Access, Terminals, Transmission and Multiplexing (ATTM).

The present document contains information on the European requirements for Very High Speed Digital Subscriber Line Systems (VDSL2). Unless specifically stated in the present document, the requirements are given in the ITU-T Specification G.993.2 (Very high speed digital subscriber line transceivers 2) [1].

# 1 Scope

The present document provides the necessary adaptions to ITU-T Recommendation G.993.2 [1] for European applications and other information relevant to the European environment.

# 2 References

References are either specific (identified by date of publication and/or edition number or version number) or non-specific.

- For a specific reference, subsequent revisions do not apply.
- Non-specific reference may be made only to a complete document or a part thereof and only in the following cases:
  - if it is accepted that it will be possible to use all future changes of the referenced document for the purposes of the referring document;
  - for informative references.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

For online referenced documents, information sufficient to identify and locate the source shall be provided. Preferably, the primary source of the referenced document should be cited, in order to ensure traceability. Furthermore, the reference should, as far as possible, remain valid for the expected life of the document. The reference shall include the method of access to the referenced document and the full network address, with the same punctuation and use of upper case and lower case letters.

NOTE: While any hyperlinks included in this clause were valid at the time of publication ETSI cannot guarantee their long term validity.



## 2.1 Normative references

The following referenced documents are indispensable for the application of the present document. For dated references, only the edition cited applies. For non-specific references, the latest edition of the referenced document (including any amendments) applies.

[1] ITU-T Recommendation G.993.2: "Very high speed digital subscriber line transceivers 2 (VDSL2)", February 2006 + Amendments and corrigenda.

[2] ETSI TS 101-388 (V1.4.1): "Access Terminals Transmission and Multiplexing(ATTM); Access transmission systems on metallic access cables; Asymmetric Digital Subscriber Line (ADSL) - European specific requirements (ITU-T Recommendation G992.1 modified)".

[3] ITU-T Recommendation G.227: "Conventional Telephone Signal", November 1988.

## 2.2 Informative references

The following referenced documents are not essential to the use of the present document but they assist the user with regard to a particular subject area**.** For non-specific references, the latest version of the referenced document (including any amendments) applies.

[i.1] [I-1] ETSI ATTM TM6 Permanent Document TM6(97) 02, June 1998, Cable reference models for simulating metallic access networks.

# 3 Definitions, symbols and abbreviations

## 3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

**crest factor (CF):** peak to rms voltage ratio

**design impedance ($R_V$):** target input and output impedance of the VDSL2 modem

NOTE: This is set at 100 Ω in [1].

**downstream:** transmission in the direction of LT towards NT (network to customer premise)

**FTTCab:** used to define when VDSL2 LT transceivers are located physically at a node (normally the Cabinet or PCP) in the periphery of the access network

**FTTEx:** used to define when VDSL2 LT transceivers are located physically at the serving Local Exchange

**reference impedance ($R_N$):** chosen impedance used for specifying transmission and reflection characteristics of cables and test loops

NOTE: ETSI has normalized this value at 135 Ω for a wide range of xDSL performance and conformance tests, including ADSL tests. This value is considered as being a reasonable average of characteristic impedances ($Z_0$) observed for a wide range of commonly used European distribution cables.

**r.m.s:** root mean square value

**upstream:** transmission in the direction of NT towards LT (customer premise to network)

**xDSL:** generic term covering the family of all DSL technologies, e.g. HDSL, SDSL, ADSL, VDSL2

## 3.2 Symbols

For the purposes of the present document, the following symbols apply:

$f_T$ Test loop calibration frequency for setting the insertion loss of the loop
kbps kilo-bits per second

NOTE: 1 kbps = 1 000 bits per second.

Mbps Mega bits per second

NOTE: 1 Mbps = 1 000 kbps.

$R_N$ Reference Impedance

NOTE: Used for specifying transmission and reflection characteristics of cables and test loops.

$R_V$ VDSL2 source/load design impedance (purely resistive)
$Z_0$ Characteristic impedance of the test loop
$Z_M$ Compromise reference impedance for the VDSL2 splitter (usually complex)

## 3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ADSL Asymmetric DSL
AM Amplitude Modulation

| | |
|---|---|
| BER | Bit Error Ratio |
| CF | Crest Factor |
| CO | Central Office |
| CP | Customer Premises |
| DC | Direct Current |
| DSL | Digital Subscriber Line (or Loop) |
| FEXT | Far End Cross Talk |
| FTTCab | Fibre To The Cabinet (see definitions) |
| FTTEx | Fibre To The Exchange (see definitions) |
| HDSL | High speed Digital Subscriber Line |
| HF | High Frequency |
| LT | Line Termination |
| LTU | Line Termination Unit |
| NEXT | Near-end crosstalk |
| NT | Network Termination |

NOTE: At the customer premise end of the line.

| | |
|---|---|
| NTU | Network Termination Unit |
| PCP | Primary Cross-connection Point |

NOTE: Also known as the cabinet.

| | |
|---|---|
| PDF | Probability Density Function |
| PEP | Psophometric Electrical Power |
| PSD | Power Spectral Density |
| PRBS | Pseudo Random Bit Sequence |
| PVC | Poly Vinyl Chloride |
| RF | Radio Frequency |
| RFI | Radio Frequency Interference |
| RMS | Root Mean Square |
| SDSL | Single pair (or Symmetric) Digital Subscriber Line |
| SW | Short Wave |
| TBD | To Be Decided |
| UPBO | Upstream Power Back-Off |
| VDSL2 | Very high speed Digital Subscriber Line 2 |

NOTE: Specified in ITU-T Recommendation G.993.2 [1].



# 4 Endorsement notice

All elements of the ITU Recommendation G.993.2 [1] apply. The European specific requirements are given in ITU-T Recommendation G.993.2 annex B [1].

# 5 Global modifications to ITU-T Recommendation G.993.2

| Terminology and Nomenclature in ITU-T Recommendation G.993.2 [1] | Terminology and Nomenclature as Modified by TS 101 271 |
|---|---|
| Central Office | Network Side |
| VTU-O | LTU |
| VTU at the Central Office | Line Termination Unit |
| VTU-R | NTU |
| VTU at the Remote End | Network Termination Unit |

# Annex ZA.1 (normative): Test Procedures

This clause provides a specification of the test set-up, the insertion path and the definition of signal and noise levels. The tests focus on the noise margin when VDSL2 signals under test are attenuated by standard test-loops and suffer interference from standard crosstalk noise or impulse noise. This noise margin indicates what increase of crosstalk noise or impulse noise level can be tolerated by the VDSL2 system under test before the bit error ratio exceeds the design target.

## ZA.1.1 Test set-up definition

Figure ZA.1 illustrates the functional description of the test set-up. It includes:

- A data source capable of generating a Pseudo Random Bit Sequence (PRBS) with a minimum length of $2^{15}$-1 to the transmitter in the direction under test at the bitrate required. The transmitter in the opposite direction shall be fed with a similar PRBS signal, although there is no need to monitor the receiver output in this path.
- The test loops, as specified in clause ZA.1.2.
- An adding element to add the common mode and differential mode impairment noise (a mix of random, impulsive and harmonic noise), as specified in clause ZA.1.3.
- An impairment generator, as specified in clause ZA.1.3, to generate both the differential mode and common mode impairment noise to be fed to the adding element.
- A high impedance and well balanced differential voltage probe (e.g. better than 60 dB across the whole VDSL2 bandwidth) connected with level detectors such as a spectrum analyzer or a true rms voltmeter.
- A high impedance and well balanced common mode voltage probe (e.g. better than 60 dB across the whole VDSL2 bandwidth) connected with level detectors such as a spectrum analyzer or a true rms voltmeter.



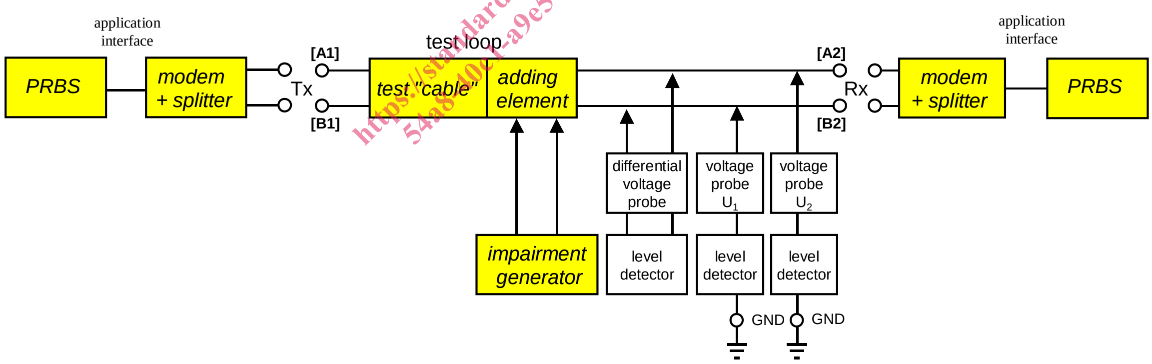


**Figure ZA.1: Functional description of the set-up of the performance tests**

The two-port characteristics (transfer function, impedance) of the test-loop, as specified in clause ZA.1.2, is defined between port Tx (node pairs A1, B1) and port Rx (node pair A2, B2). The consequence is that the two-port characteristics of the test "cable" in figure ZA.1 must be properly adjusted to take full account of non-zero insertion loss and non-infinite shunt impedance of the adding element and impairment generator. This is to ensure that the insertion of the generated impairment signals does not appreciably load the line.

The balance about earth, observed at both ports and at the tips of the voltage probe shall exhibit a value that is 10 dB greater than the transceiver under test. This is to ensure that the impairment generator and monitor function does not appreciably deteriorate the balance about earth of the transceiver under test.

The signal flow through the test set-up is from port Tx to port Rx, which means that measuring upstream and downstream performance requires an interchange of transceiver position and test "cable" ends.

The received signal level at port Rx is the level, measured between node A2 and B2, when port Tx as well as port Rx are terminated with the VDSL2 transceivers under test. The impairment generator is switched off during this measurement.

Test Loop #0, as specified in clause ZA.1.2, shall always be used for calibrating and verifying the correct settings of generators G1-G7, as specified in clause ZA.1.3, during performance testing.

The transmitted signal level at port Tx is the level, measured between node A1 and B1, under the same conditions.

The impairment noise shall be a mix of random, impulsive and harmonic noise, as defined in clause ZA.1.3. The level that is specified in clause ZA.1.3 is the level at port Rx, measured between node A2 and B2, while port Tx as well as port Rx are terminated with the design impedance RV. These impedances shall be passive when the transceiver impedance in the switched-off mode is different from this value.

### ZA.1.1.1 Signal and noise level definitions

The signal and noise levels are probed with a well balanced differential voltage probe ($U_2$-$U_1$). The differential impedance between the tips of that probe shall be higher than the shunt impedance of 100 kΩ in parallel with 10 pF. Figure ZA.1 shows the probe position when measuring the Rx signal level at the LT or NT receiver. Measuring the Tx signal level requires the connection of the tips to node pair (A1, B1).

The common mode signal and noise levels are probed with a well balanced common mode voltage probe as the voltage between nodes A2, B2 and ground. Figure ZA.1 shows the position of the two voltage probes when measuring the common mode signal. The common mode voltage is defined as $1/2(U_1+U_2)$.

NOTE: The various levels (or spectral masks) of signal and noise that are specified in the present document are defined at the Tx or Rx side of this set-up. The various levels are defined while the set-up is terminated, as described above, with the design impedance $R_V$ or with VDSL2 transceivers under test.

Probing an rms-voltage Urms (V) in this set-up, over the full signal band, means a power level of P (dBm) that equals:

$P = 10 \times \log_{10} (U_{rms}^2/R_V \times 1\,000)$ dBm

Probing an rms-voltage Urms (V) in this set-up, within a small frequency band of Δf (in Hertz), means an average spectral density level of P (dBm/Hz) within that filtered band that equals:

$P = 10 \times \log_{10} (U_{rms}^2/R_V \times 1\,000/\Delta f)$ (dBm/Hz)

The bandwidth Δf identifies the noise bandwidth of the filter, and not the -3 dB bandwidth.



## ZA.1.2 Test loops

The purpose of the test loops shown in figure ZA.2 is to stress VDSL2 transceivers under a wide range of different conditions that can be expected when deploying VDSL2 in real networks.

### ZA.1.2.1 Functional description

The test loops in this clause are an artificial mixture of cable sections. A number of different loops have been used to represent a wide range of cable impedances, and to represent ripple in amplitude and phase characteristics of the test loop transfer function.

- The physical length of the individual loops is to be chosen such that the transmission characteristics of all loops are comparable. This is achieved by normalizing the *electrical* length of the loops (insertion loss at 300 kHz). The purpose of this is to stress the equalclauser of the VDSL2 modem under test in a similar way over all loops, when testing at a specific bitrate.

The loops are defined as a combination of cable sections. Each section is defined by means of two-port cable models of the individual sections (see annex ZA.2). Cable simulators as well as real cables can be used for these sections.

- Loop #0 is a symbolic name for a loop with zero (or near zero) length, to prove that the VDSL2 transceiver under test can handle the potentially high signal levels when two transceivers are directly interconnected.

- The impedances of Loop #1 and #2 are nearly constant over a wide frequency interval. These two loops represent uniform distribution cables, one having a relatively low characteristic impedance and another having a relatively high impedance (low capacitance per unit length). These impedance values are chosen to be the lowest and highest values of distribution cables that are commonly used in Europe.
- The impedances of Loop #3 and #4 follow frequency curves that are oscillating in nature. This represents the mismatch effects in distribution cables caused by a short extent with a cable that differs significantly in characteristic impedance. Loop #3 represents this at the LT side to stress downstream signals. Loop #4 does the same at the NT side to stress upstream signals.

Test loops 1 to 4 in figure ZA.2 have equal *electrical* length (insertion loss at 300 kHz), but differ in input impedance (see figure ZA.3). It is these values for insertion loss and impedance that define an actual test loop set. This clause only defines the loop topology – the detailed loop lengths are out of scope for the present document.

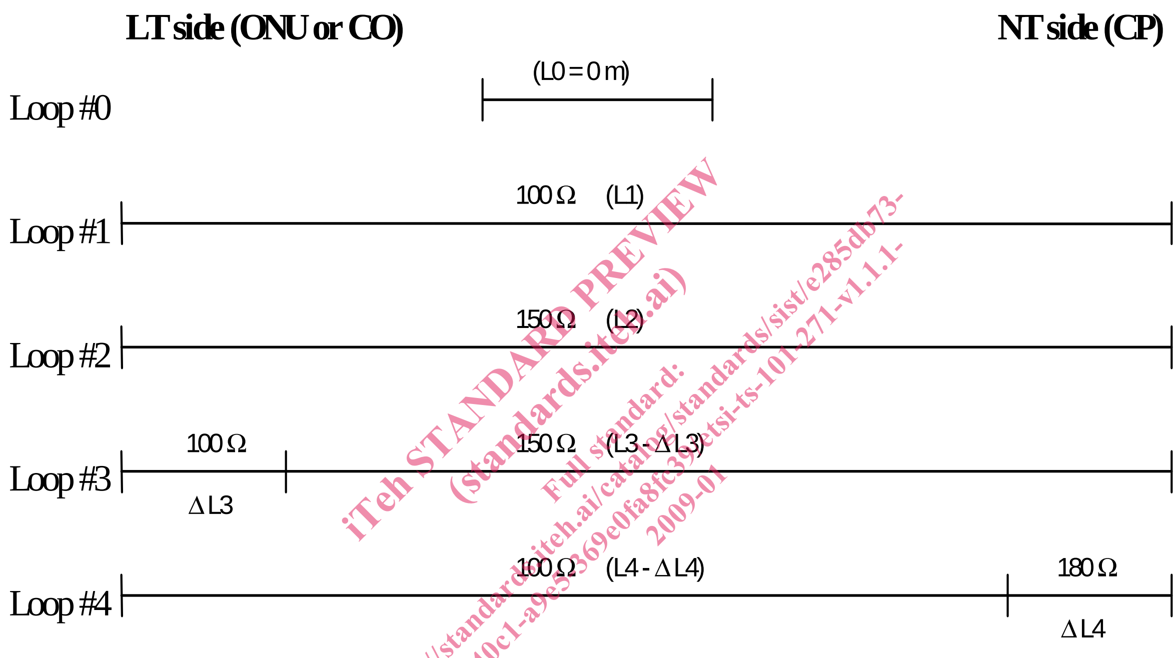




**Figure ZA.2: Test loop topology**

The physical composition of the various test loops is defined in table ZA.1.

**Table ZA.1: Test loop composition**

| Test loop | Distribution cable (L) | Extension cable (ΔL) LT or NT side | Extension length ΔL [m] |
|---|---|---|---|
| **#0** | - | - | - |
| **#1** | TP100 | - | - |
| **#2** | TP150 | - | - |
| **#3** | TP150 | TP100x | 70 |
| **#4** | TP100 | TP180x | 70 |
| NOTE: The labels "TPxxx" refer to the two-port cable models specified in annex ZA.2. | | | |

The variation of input impedance for the various test loops is shown in figure ZA.3. Some typical transfer functions of loops #1 to #4 are illustrated in figure ZA.4. The test loops in this example are normalized in *electrical* length (or insertion loss) at an arbitrary chosen frequency. Five examples denoted by Q1 to Q5 are shown in figure ZA.4. Loop-set Q1 has an insertion loss of 55 dB at 2 MHz and loop-set Q5 has an insertion loss of 18,5 dB at 10 MHz. The *physical* length of loop-set Q1 is in the range of 1 990 m to 2 100 m and for loop-set Q5 is in the range of 250 m to 300 m. The plot demonstrates the similarity of the transfer function of all the different loops when they are normalized.

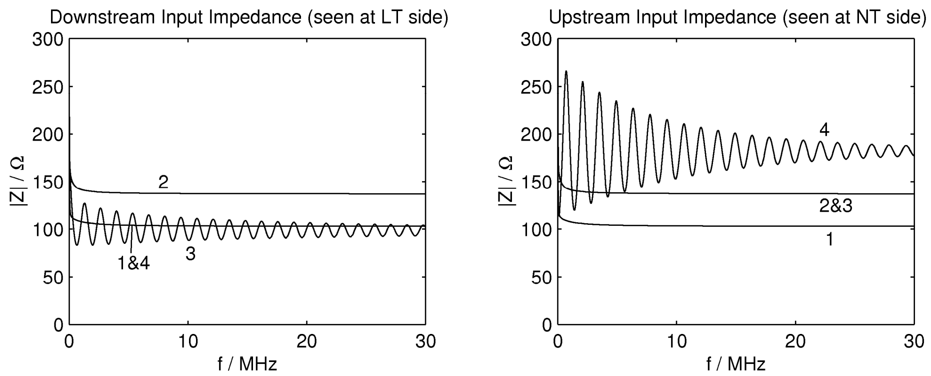


**Figure ZA.3: Calculated variation of input impedance at a normalized loop length of 5 000 m**

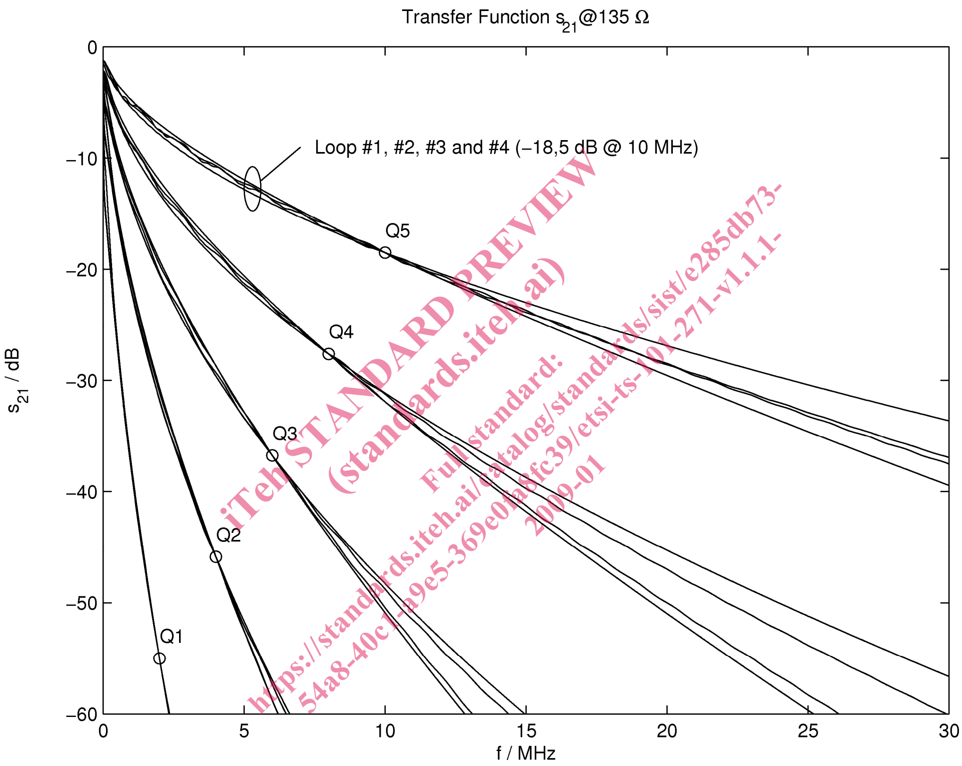




**Figure ZA.4:Typical transfer function (in $R_N$=135 Ω)**
**of the test loops when normalized in electrical length**

The sections of the loops are defined in annex ZA.2 by means of two-port cable models of the individual sections. Cable simulators as well as real cables can be used for these sections. To minimize the electrical differences between test loop configurations, their length is specified as *electrical* lengths instead of the physical length of the sections in cascade (meaningful only when real cables are used). The electrical length is equivalent to the insertion loss of the loop at a given test frequency and termination impedance.

The relationship between *electrical* length (insertion loss) and total *physical* length (when real cables are used) can be calculated from the two-port models given in annex ZA.2.

## ZA.1.2.2 Test loop accuracy

The different cable sections are specified by two-port cable models that serve as a representation for real twisted-pair cables. Cable simulators as well as real cables can be used for these test loops. The associated models and line constants are specified in annex ZA.2. The composition of the test-loops is specified in table ZA.1.