TECHNICAL REPORT

ISO/IEC TR 15294

First edition
2000-04-01

Information technology — Methods for data flow control at synchronous and asynchronous DTE-DCE interfaces

Technologies de l'information — Méthodes pour interfaces DTE-DCE synchrones et asynchrones de commande de flux de données

Reference number
ISO/IEC TR 15294:2000(E)

ISO copyright office
Case postale 56 • CH-1211 Geneva 20
Tel. + 41 22 749 01 11
Fax + 41 22 734 10 79
E-mail copyright@iso.ch
Web www.iso.ch

Printed in Switzerland

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 3.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

In exceptional circumstances, when a technical committee has collected data of a different kind from that which is normally published as an International Standard ("state of the art", for example), it may decide by a simple majority vote of its participating members to publish a Technical Report. A Technical Report is entirely informative in nature and does not have to be reviewed until the data it provides are considered to be no longer valid or useful.

Attention is drawn to the possibility that some of the elements of this Technical Report may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

ISO/IEC TR 15294, was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 6, *Telecommunications and information exchange between systems*.

This Technical Report is technically aligned with ITU-T Recommendation V.43, but is not published as identical text.

Introduction

When using DCEs incorporating data compression and/or error correction, it is essential that the DCE have some method of controlling the flow of data from the DTE (a similar requirement applies for the associated DTEs, see below). This is because the degree of compression obtained will vary from moment to moment, and the buffers in the DCE may fill up during periods of lower compression, or while correction of transmission errors is active.

Likewise, during periods of high compression, the DTE may become overloaded with the amount of incoming data and may not be able to process this data properly without means of controlling the flow of data from the DCE.

There are many methods of flow control in existence, and DCE and DTE designers should ensure that they provide methods suitable for the associated DTE and DCE, respectively, to be used.

This Recommendation aims at giving guidelines in order to assist DTE and DCE designers in their tasks. It lists several mechanisms which are known to operate successfully with DTEs and DCEs although no single mechanism will operate with all DTEs and DCEs, and some DTEs may not respond to any of the mechanisms described. Both the synchronous and the asynchronous modes of operation are addressed.

NOTE The guidelines given in this Technical Report may not be exhaustive.

Information technology — Methods for data flow control at synchronous and asynchronous DTE-DCE interfaces

1 Scope

This Technical Report provides guidance for the choice of an appropriate method for, and the implementation of, data flow control capabilities in DTEs and DCEs. It also coordinates information from other Recommendations and International Standards and provides tutorial material on these flow control techniques.

2 Reference

[1] ITU-T Recommendation V.24, *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment.*

3 Abbreviation

IRA International reference alphabet

4 Data Flow Control Methods

The guidance is provided for

— flow control of transmitted data,

— flow control of received data.

each of which is subdivided according to asynchronous and synchronous modes of operation. It is assumed that the asynchronous mode of operation in the context of this Technical Report is accomplished using synchronous DCEs incorporating asynchronous-to-synchronous conversion according to e.g. Recommendation V.14 or V.42.

This Technical Report restricts itself to the description of methods for flow control that exist locally between a DTE and a DCE. Methods for end-to-end flow control involving the two DTEs or the two DCEs concerned are beyond the scope of this Technical Report.

At present this Technical Report describes only flow control methods that operate at the physical layer of the OSI Reference Model. In the context of this Technical Report, the use of DC1/DC3 characters is also understood as to fall in this category. Methods that involve the DCE implementing layer 2 or higher layer protocols, for example HDLC, are for further study.

4.1 Methods for flow control of transmitted data

The control function of the DCE shall be capable of indicating to the DTE a temporary inability to accept data on circuit 103, Transmitted Data (DCE not-ready condition). Upon receiving such an indication, the DTE shall ideally complete transmission of any partially transmitted character (asynchronous mode of operation) or frame (synchronous mode of operation) and then cease transmitting data on circuit 103 and clamp circuit 103 to binary 1. When the DCE not-ready condition is cleared, the DTE may resume the transmission of data on circuit 103.

Figure 1 depicts the interchange circuits at the DTE-DCE interface and the functionalities inside the DTE and the DCE, respectively, which may be used, as appropriate, for the flow control of transmitted data.

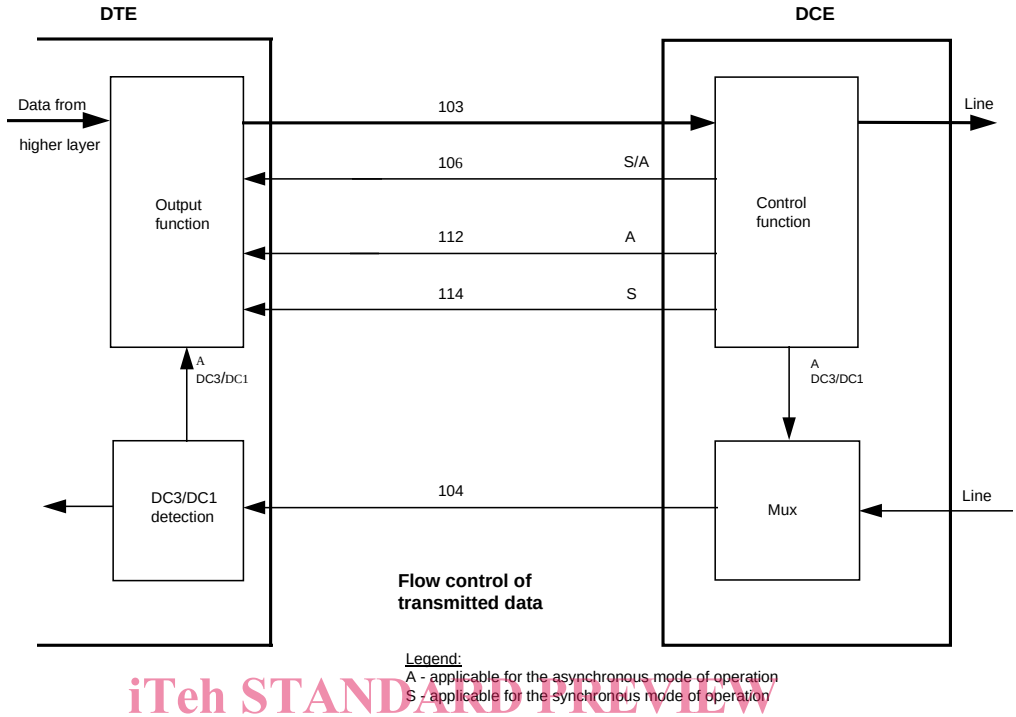

Figure 1

4.1.1 Asynchronous mode of operation

Two standard methods exist:

4.1.1.1 Flow control by use of V.24 interchange circuits

a) Use of circuit 106 - Ready for sending

The DCE not-ready condition is indicated by turning circuit 106 OFF, and cleared by turning circuit 106 ON.

This method should be the preferred one because it is unambiguous and is applicable to any kind of data communication. However, many DTEs will not immediately recognize the OFF condition on circuit 106 and will not cease transmitting at the end of the present character. Instead, these DTEs will complete the present frame which may be up to some thousand octets long, and only then detect the OFF condition on circuit 106.

It is therefore suggested that the remaining buffer capacity inside the DCE be kept large enough to cope with this condition. A reasonable remaining buffer size suggested may be between 2,000 and 4,000 octets, so that the minimum total buffer size may be between 4,000 octets (DCE not-ready condition is indicated to the DTE when the buffer is half-full) and 10,000 octets (DCE not-ready condition is indicated to the DTE when about 80 % of the buffer is full).

NOTE This assumes that a remaining buffer size of about 2,000 octets is needed.

For a DTE to be able to interwork with DCEs incorporating data compression and/or error correction it is advisable that the DTE cyclically check the condition of circuit 106 and, upon recognition of the OFF condition on circuit 106, stop the transmission of data as soon as possible.

b) Use of circuit 112 - Data signalling rate selector (DCE source)

The DCE may, by controlling circuit 112, select one of two data signalling rates in the DTE to coincide with the data signalling rate in use in the DCE.

The ON condition on this circuit selects the higher rate, the OFF condition selects the lower rate.

4.1.1.2 Flow control by use of DC3/DC1 characters

The DCE not-ready condition is indicated by transmitting a DC3 character (IRA character 1/3), and cleared by transmitting a DC1 character (IRA character 1/1), on circuit 104.

This method should not be applied when there is a risk that binary characters that appear in the data stream may be confused with DC3 and DC1 characters, which would result in a malfunction of the system.

Schemes that indicate in binary file transfer whether a DC3 or a DC1 character that the DTE detects in the data transmitted on circuit 104 either is generated by the DCE for the purpose of flow control, or is a binary character and part of the data received from the remote DTE, are for further study.

4.1.2 Synchronous mode of operation

A variety of methods is conceivable for the synchronous mode of operation.

4.1.2.1 Flow control by changing the rate of the transmitter signal element timing (DCE source)

When the transmit clock signal is sourced from the DCE (circuit 114), it may be possible to slow the data flow from the DTE by reducing the clock rate. The clock rate should be halved by the DCE and, if that action is insufficient, the rate should be halved again, and so on. The clock rate should be increased again as soon as conditions in the DCE have improved.

The change to a different rate has to occur while circuit 114 is in the OFF condition.

NOTE Some DTEs use narrow-band phase-locked loops in their received clock circuitry and may not be able to respond to this mechanism.

4.1.2.2 Flow control by stopping the transmitter signal element timing signal (DCE source)

This method halts the clock signal on circuit 114, thus causing the DTE to stop sending. Circuit 114 may be held in the OFF condition for a limited period of time. The duration of the OFF condition shall be an integer multiple of the length of a signal element at the normal (maximum) signalling rate. Signalling on this circuit may be resumed at a different rate, as specified above.

NOTE 1 Some DTEs may - with or without a certain time-out - raise an alarm under this condition.

NOTE 2 The recommended maximum permissible duration of an OFF condition on circuit 114 is for further study.

4.1.2.3 Flow control by use of circuit 106

Circuit 106 (Ready for sending) may be turned OFF when the buffers in the DCE are almost full (i.e. to a specified degree). This method of operation follows the definition of circuit 106 in Recommendation V.24. The considerations concerning the DCE buffer size given in subclause 4.1.1.1 a) apply.

If the transmit clock is sourced from the DTE (circuit 113), this may be the only usable method.

4.2 Methods for flow control of received data

The DTE shall be capable of indicating to the DCE a temporary inability to accept data on circuit 104, Received Data (DTE not-ready condition). Upon receiving such an indication, the DCE shall complete the delivery of any partially transmitted character (asynchronous mode of operation) or frame (synchronous mode of operation) and then cease delivering data to the DTE on circuit 104 and clamp circuit 104 to binary 1.

When the DTE not-ready condition is cleared, the DCE may resume the delivery of data on circuit 104.

NOTE The data whose flow is temporarily stopped or slowed down is originated from the remote DTE. In order to control the flow of that data so that no data is lost, the local DCE will either need to provide a received data buffer whose size cannot be specified in this Technical Report, or a mechanism will need to be implemented in the system to force the remote DTE to stop transmitting data until such time as the DTE not-ready condition is cleared.

Figure 2 depicts the interchange circuits at the DTE-DCE interface and the functionalities inside the DTE and the DCE, respectively, which may be used, as appropriate, for the flow control of received data.

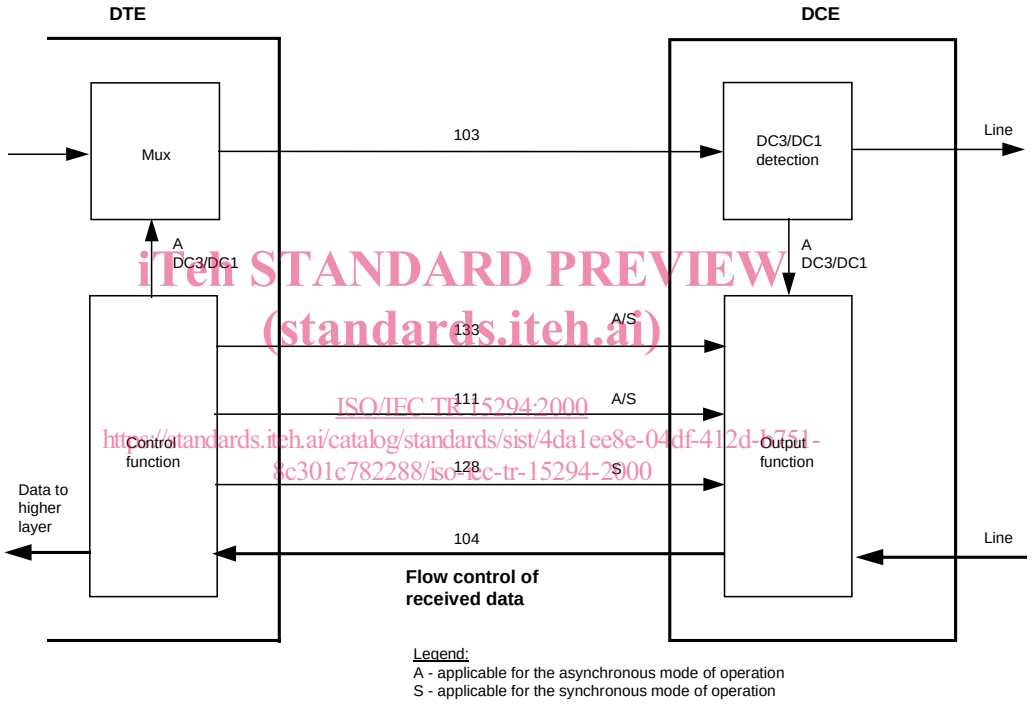

Figure 2

4.2.1 Asynchronous mode of operation

The same two standard methods exist as for the control of transmitted data:

4.2.1.1 Flow control by use of V.24 interchange circuits

a) Use of circuit 133 - Ready for receiving

The DTE not-ready condition is indicated by turning OFF circuit 133, and is cleared by turning circuit 133 ON.

This method should be the preferred one as it is unambiguous and is applicable to any kind of data communication. It may be assumed that most DCEs recognize with only a short delay the changed condition on circuit 133, and will act accordingly. The remaining buffer size in the DTE may therefore be kept small.

This method is not applicable for half-duplex protocols because circuit 105 will not be available at the DCE. The DCE will always operate in the constant carrier mode.

NOTE In many publications, circuit 133 (Ready for receiving) is, incorrectly, referred to as circuit 105 (Request to send). These two interchange circuits are significantly different in their respective definitions and functions. The source for confusion may be that, due to a lack of free poles on the interface connectors standardized in ISO/IEC 2110 and ISO/IEC 11569, both interchange circuits are allocated to the same pole (i.e. pole 4) of these connectors.

b) Use of circuit 111 - Data signalling rate selector (DTE source)

The DTE may select one of two data signalling rates of a dual rate synchronous DCE by using circuit 111. The ON condition of this circuit selects the higher rate, the OFF condition selects the lower rate.

4.2.1.2 Flow control by use of DC3/DC1 characters

The DTE not-ready condition is indicated by transmitting a DC3 character (IRA character 1/3), and cleared by transmitting a DC1 character (IRA character 1/1), on circuit 103, Transmitted Data.

This method should not be applied when there is a risk that binary characters that appear in the data stream may be confused with DC3 and DC1 characters, which would result in a malfunction of the system.

Schemes that indicate in binary file transfer whether a DC3 or a DC1 character that the DCE detects in the data it receives on circuit 103 either is generated by the DTE for the purpose of flow control, or is a binary character and part of the data to be transmitted to the remote DTE, are for further study.

4.2.2 Synchronous mode of operation

4.2.2.1 Flow control by use of V.24 interchange circuits

a) Use of circuit 133 - Ready for receiving

The DTE not-ready condition is indicated by turning OFF circuit 133, and is cleared by turning circuit 133 ON.

This method is unambiguous and is applicable to any kind of data communication. It may be assumed that most DCEs recognize with only a short delay the changed condition of circuit 133, and will act accordingly. The remaining buffer size in the DTE may therefore be kept small.

This method is not applicable for half-duplex protocols because circuit 105 will not be available at the DCE. The DCE will always operate in the constant carrier mode.

NOTE In many publications, circuit 133 (Ready for receiving) is, incorrectly, referred to as circuit 105 (Request to send). These two interchange circuits are significantly different in their respective definitions and functions. The source for confusion may be that, due to a lack of free poles on the interface connectors standardized in ISO/IEC 2110 and ISO/IEC 11569, both interchange circuits are allocated to the same pole (i.e. pole 4) of these connectors.

b) Use of circuit 111 - Data signalling rate selector (DTE source)

The DTE may select one of two data signalling rates of a dual rate synchronous DCE by using circuit 111. The ON condition of this circuit selects the higher rate, the OFF condition selects the lower rate. The DCE shall select the transmitter signal element timing (circuit 114) and the receiver signal element timing (circuit 115) accordingly.

4.2.2.2 Flow control by changing the rate of the received signal element timing (DTE source)

This method is restricted to non-standard applications where circuit 128 (Received Signal Element Timing (DTE source)) is provided in both the DTE and the DCE. For these cases, it may be possible to slow the data flow from the DCE by reducing the clock rate on circuit 128. The clock rate should be halved by the DTE and, if that action is insufficient, the rate should be halved again, and so on. The clock rate should be increased again as soon as conditions in the DTE improve. The change to a different rate shall occur while circuit 128 is in the OFF condition.